Schematic Package Supplement
to

Kangaroo™

Operation, Maintenance and Service Manual

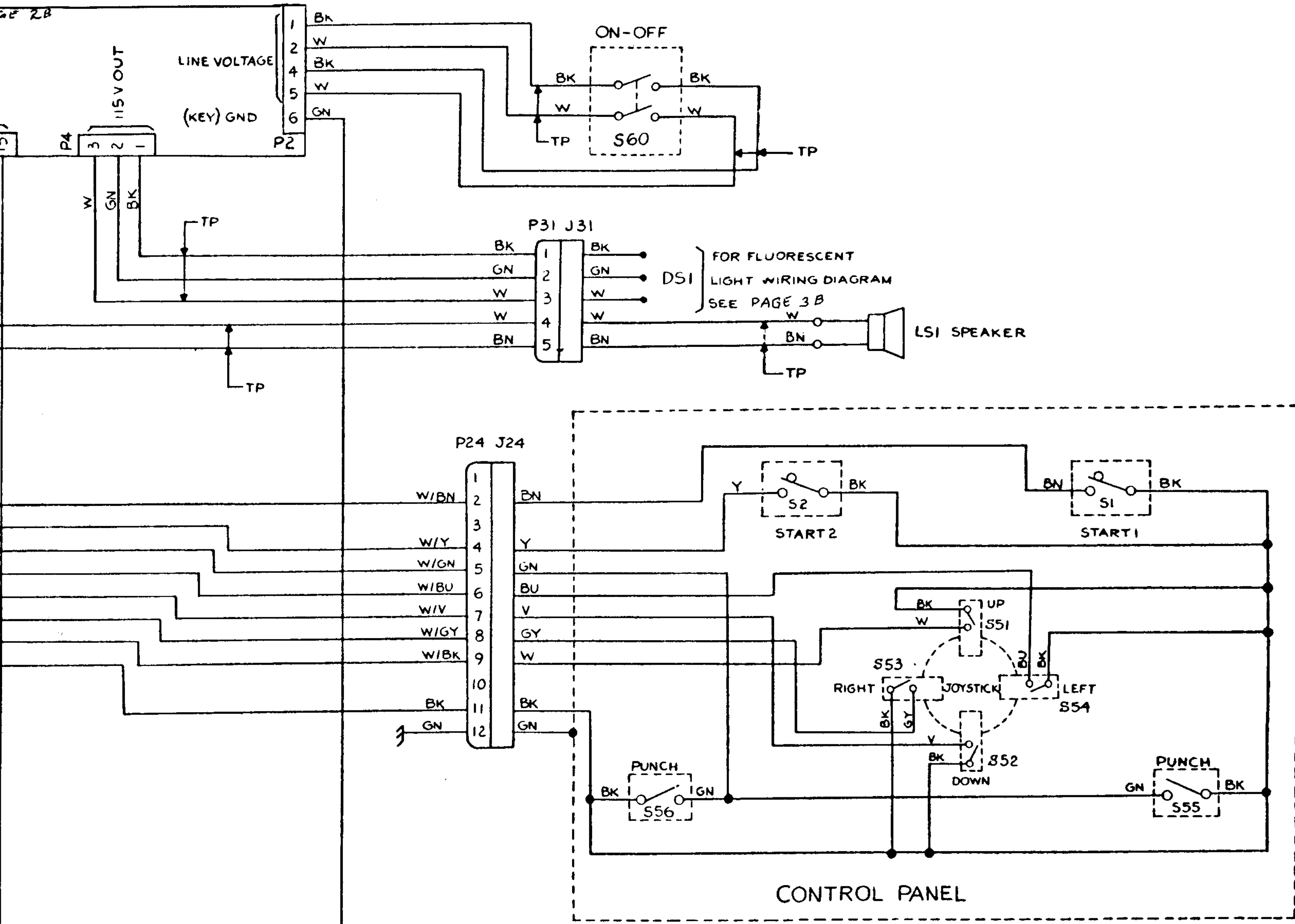
NOTE
This staple temporarily holds the schematic package together. Remove the staple before using the schematics.

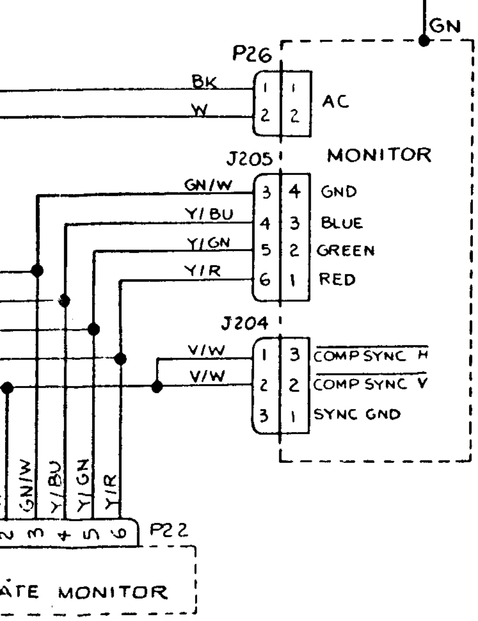
ATARI®
A Warner Communications Company

7L

SP-204 Sheet 1A
3rd printing

Table of Contents

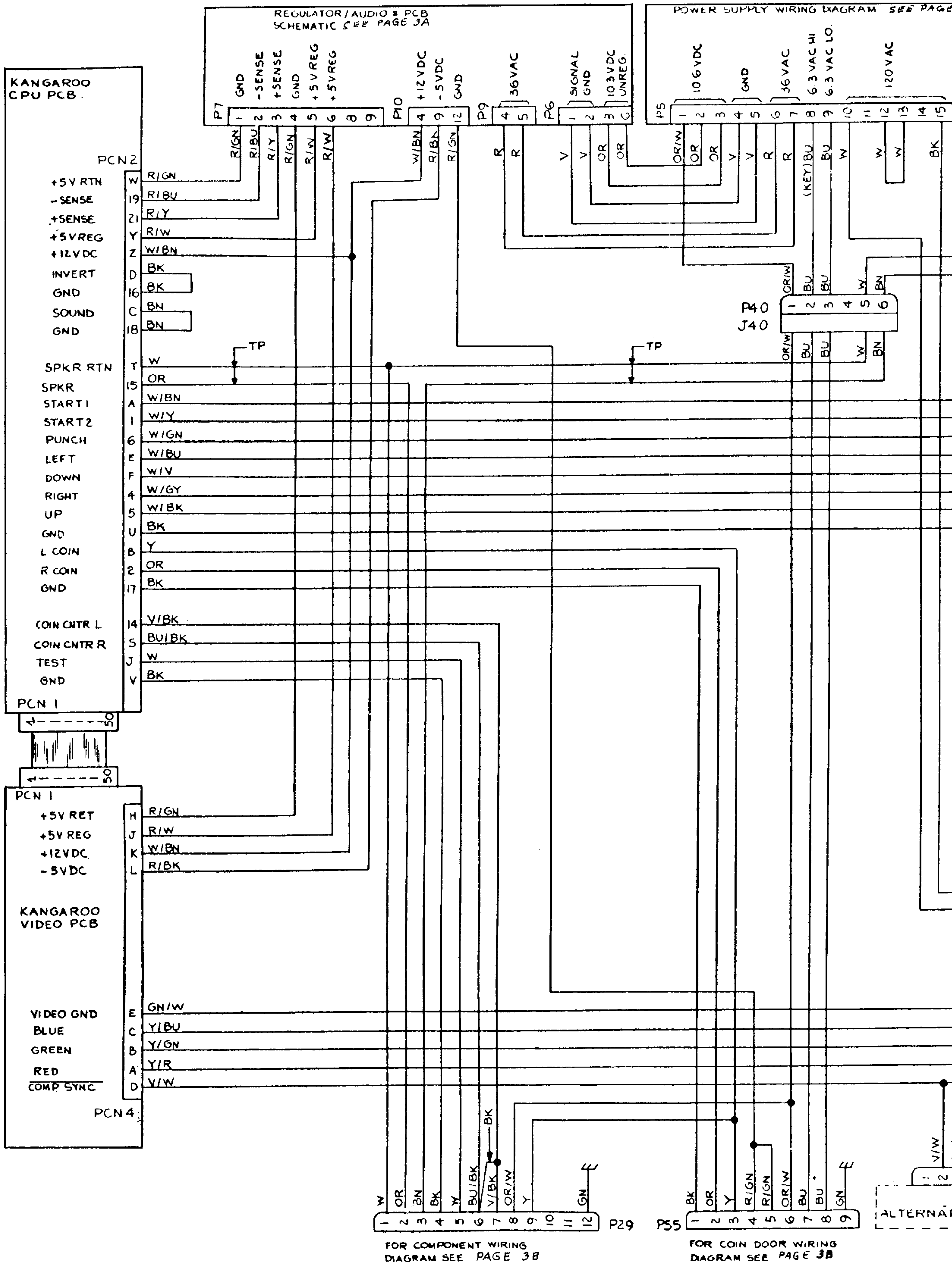




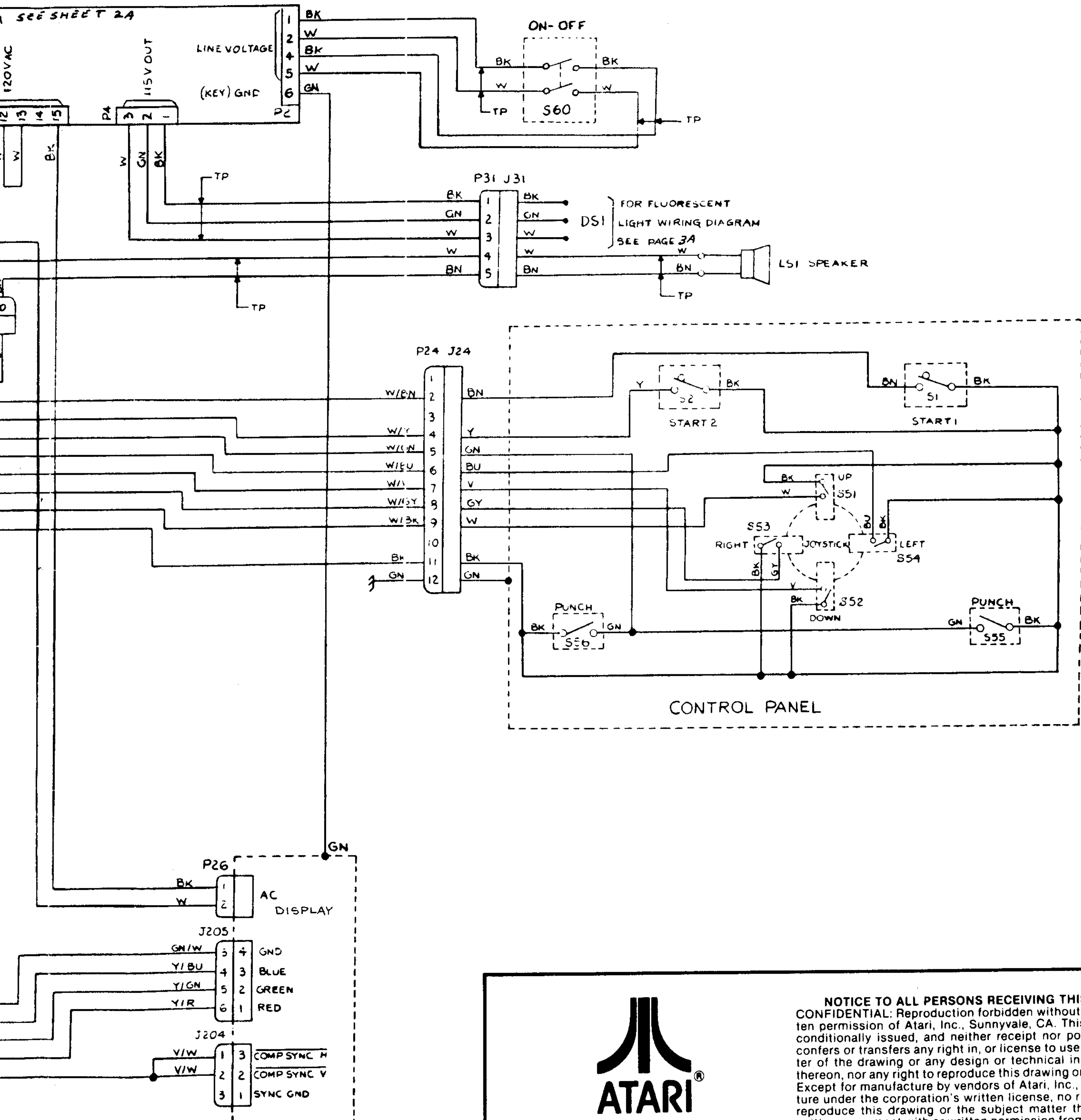
Kangaroo Upright Game Wiring Diagram

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REGULATOR / AUDIO PCB SCHEMATIC SEE PAGE 3A
POWER SUPPLY WIRING DIAGRAM SEE PAGE
KANGAROO CPU PCB
PCN2
+5V RTN
-SENSE
+SENSE
+5VREG
+12VDC
INVERT
GND
SOUND
GND
SPKR RTN
SPKR
START 1
START 2
PUNCH
LEFT
DOWN
RIGHT
UP
GND
L COIN
R COIN
GND
COIN CNTR L
COIN CNTR R
TEST
GND
PCN 1
KANGAROO VIDEO PCB
+5V RET
+5V REG
+12VDC
-5VDC
VIDEO GND
BLUE
GREEN
RED
COMP SYNC
PCN4
P7
GND
-SENSE
+SENSE
GND
+5V REG
+5V REG
P10
+12VDC
-5VDC
GND
P9
36VAC
P6
SIGNAL GND
103VDC UNREG.
P5
106VDC
GND
36VAC
6.3 VAC HI
6.3 VAC LO
120VAC
(KEY)
P40
J40
TP
TP
P29
P55
ALTERNA
FOR COMPONENT WIRING DIAGRAM SEE PAGE 3B
FOR COIN DOOR WIRING DIAGRAM SEE PAGE 3B

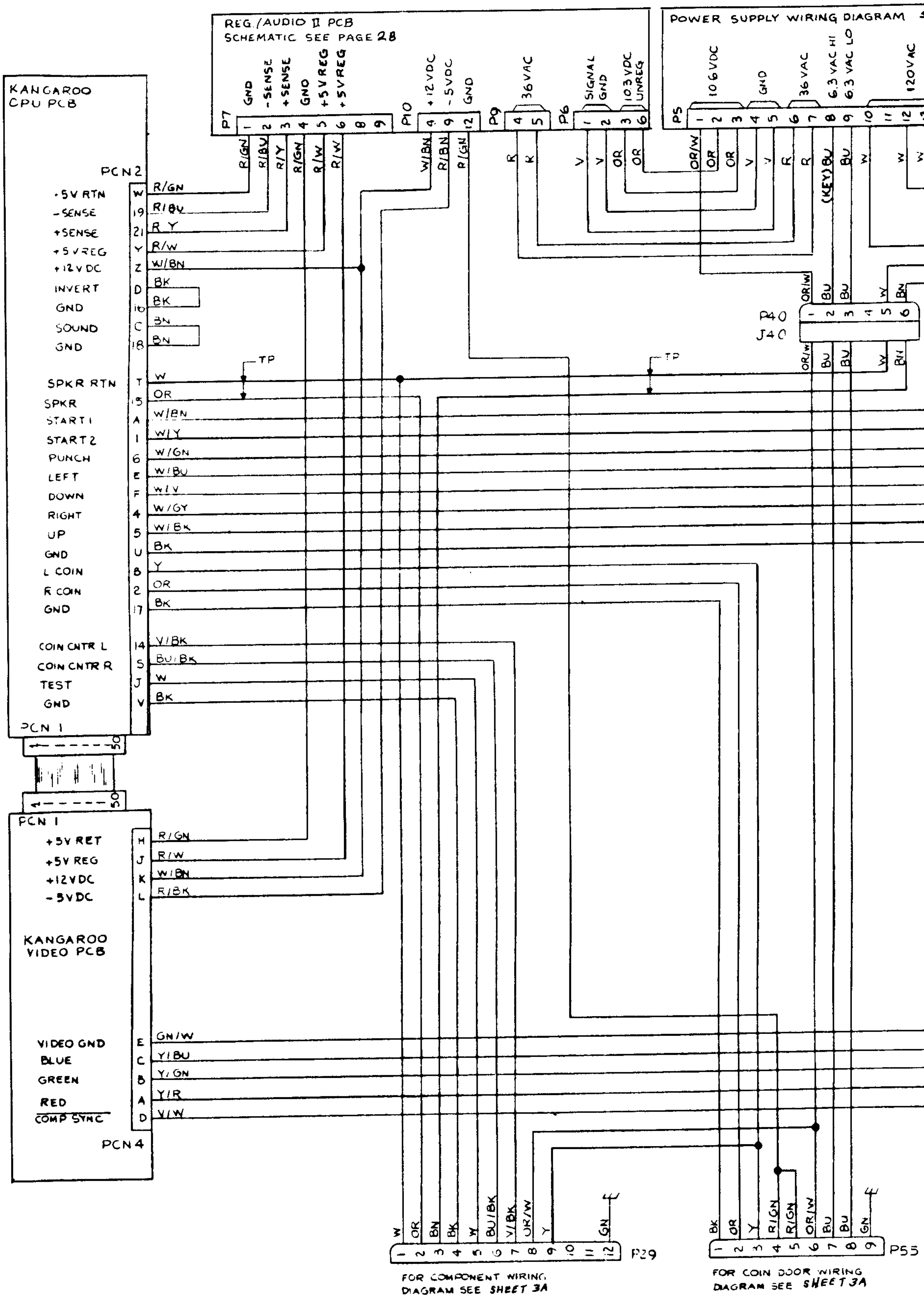


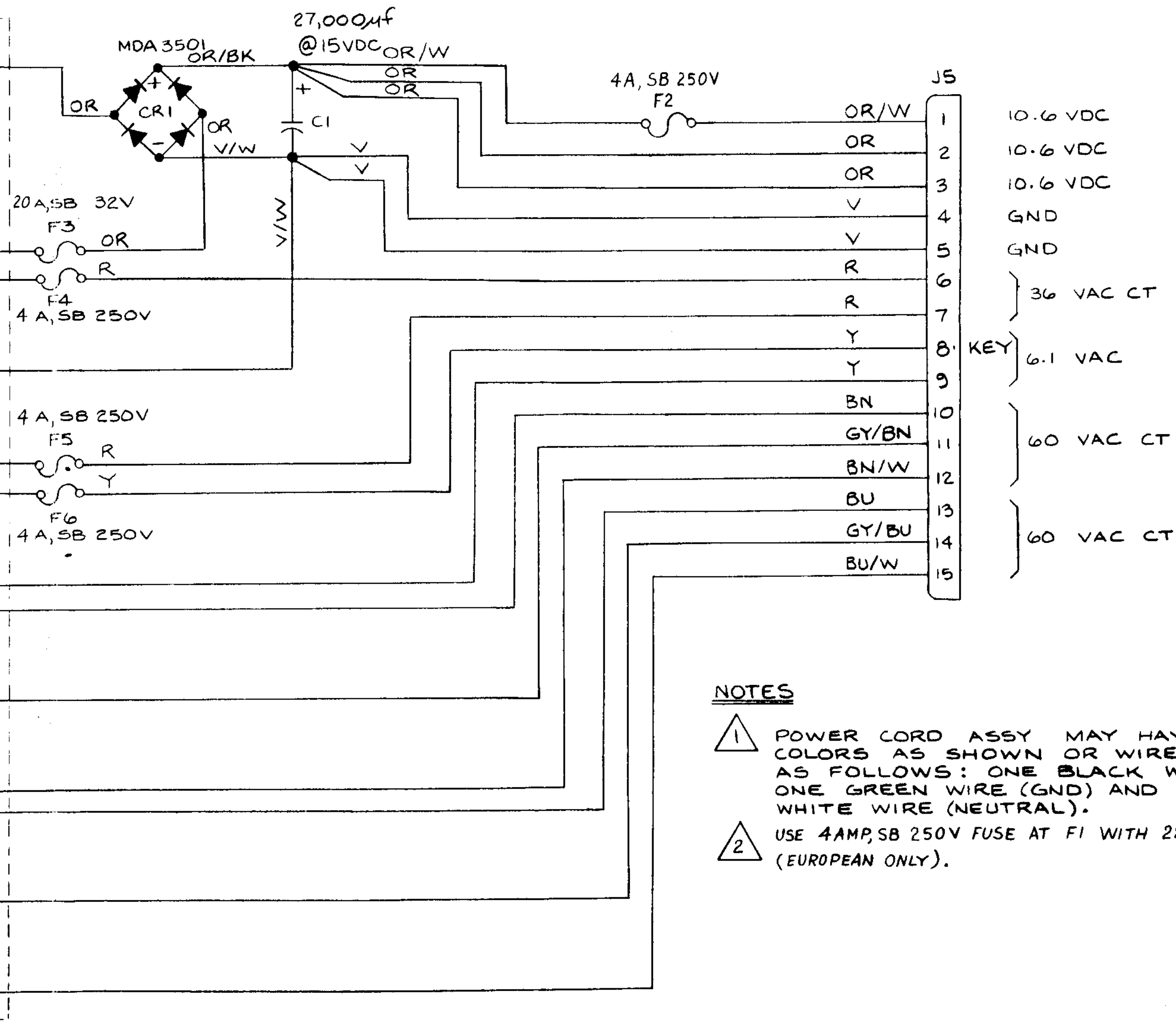
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Ireland-Built Kangaroo Game Wiring Diagram

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REG./AUDIO II PCB
SCHEMATIC SEE PAGE 28
P7
GND
-SENSE
+SENSE
GND
+5V REG
+5V REG
P10
+12VDC
-5VDC
GND
P9
36VAC
P6
SIGNAL GND
103VDC UNREG
POWER SUPPLY WIRING DIAGRAM
P5
106VDC
GND
36VAC
6.3VAC HI
6.3VAC LO
120VAC
(KEY)BU
P40
J40
TP
TP
KANGAROO CPU PCB
PCN2
+5V RTN
-SENSE
+SENSE
+5VREG
+12VDC
INVERT
GND
SOUND
GND
SPKR RTN
SPKR
START 1
START 2
PUNCH
LEFT
DOWN
RIGHT
UP
GND
L COIN
R COIN
GND
COIN CNTR L
COIN CNTR R
TEST
GND
PCN 1
PCN 1
+5V RET
+5V REG
+12VDC
-5VDC
KANGAROO VIDEO PCB
VIDEO GND
BLUE
GREEN
RED
COMP SYNC
PCN4
P29
FOR COMPONENT WIRING DIAGRAM SEE SHEET 3A
P55
FOR COIN DOOR WIRING DIAGRAM SEE SHEET 3A



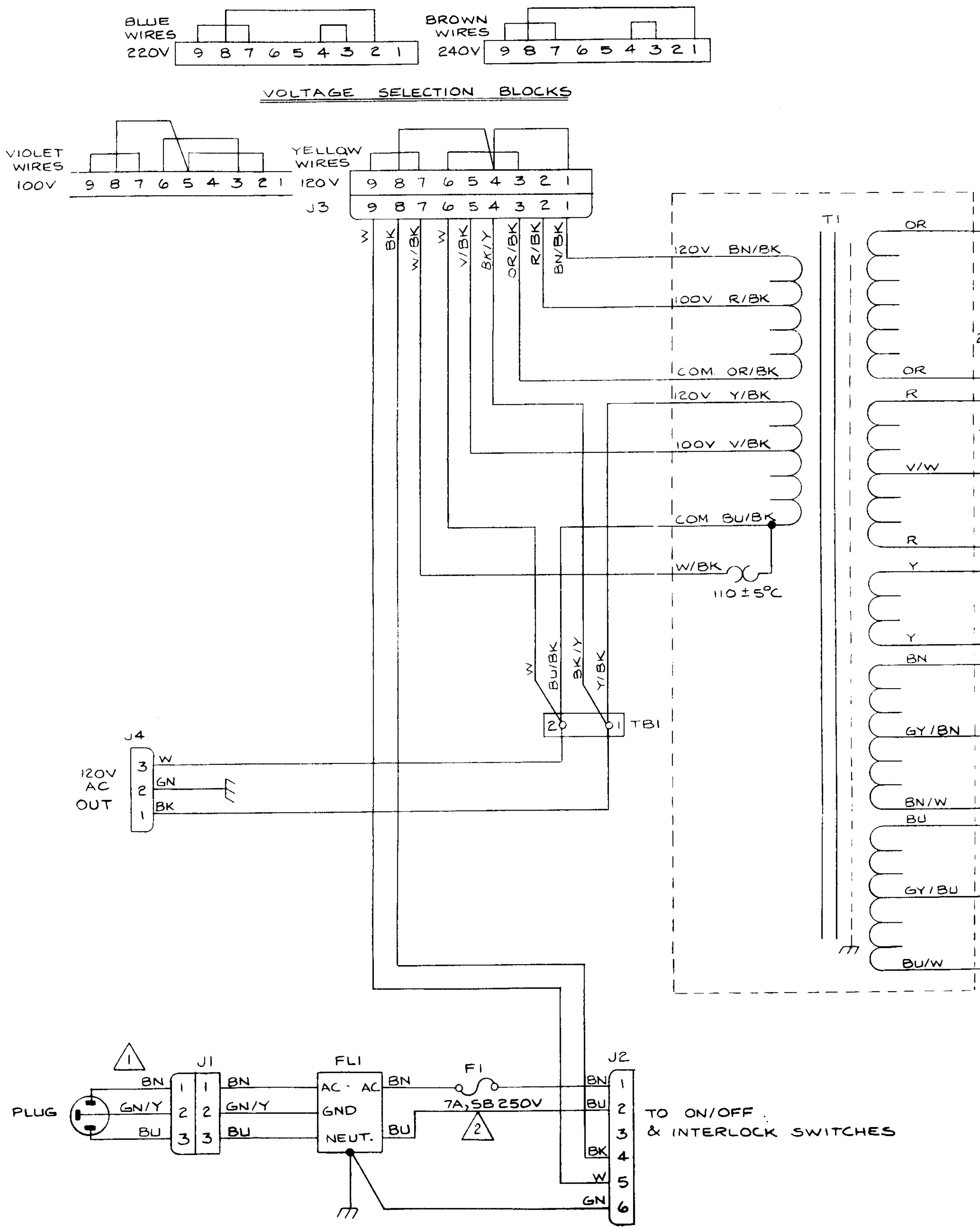
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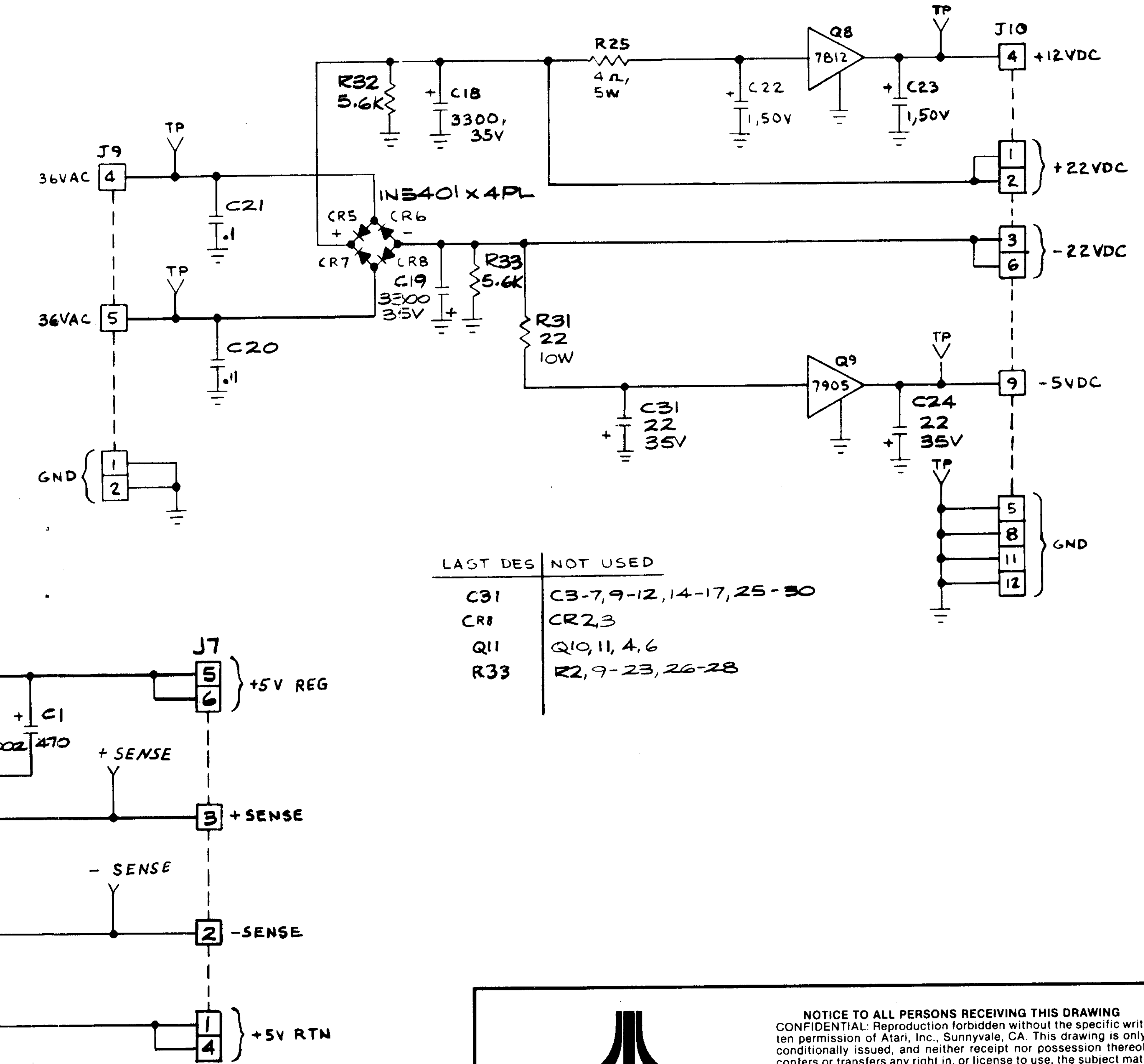
1. POWER CORD ASSY MAY HAVE WIRE COLORS AS SHOWN OR WIRE COLORS AS FOLLOWS: ONE BLACK WIRE (AC), ONE GREEN WIRE (GND) AND ONE WHITE WIRE (NEUTRAL).
2. USE 4AMP, SB 250V FUSE AT F1 WITH 220V & 240V (EUROPEAN ONLY).

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Kangaroo Power Supply

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BLUE WIRES
220V
9 8 7 6 5 4 3 2 1
BROWN WIRES
240V
9 8 7 6 5 4 3 2 1
VOLTAGE SELECTION BLOCKS
VIOLET WIRES
100V
9 8 7 6 5 4 3 2 1
YELLOW WIRES
120V
9 8 7 6 5 4 3 2 1
J3
9 8 7 6 5 4 3 2 1
W
BK
W/BK
W
V/BK
BK/Y
OR/BK
R/BK
BN/BK
T1
120V BN/BK
100V R/BK
COM. OR/BK
120V Y/BK
100V V/BK
COM BU/BK
W/BK
110 ± 5°C
OR
OR
R
V/W
R
Y
Y
BN
GY/BN
BN/W
BU
GY/BU
BU/W
W
BU/BK
BK/Y
Y/BK
2
1
TB1
J4
120V AC OUT
3 W
2 GN
1 BK
PLUG
BN
GN/Y
BU
J1
1 1
2 2
3 3
BN
GN/Y
BU
FL1
AC · AC
GND
NEUT.
BN
BU
F1
7A, SB 250V
2
1
J2
BN 1
BU 2
3
BK 4
W 5
GN 6
TO ON/OFF & INTERLOCK SWITCHES



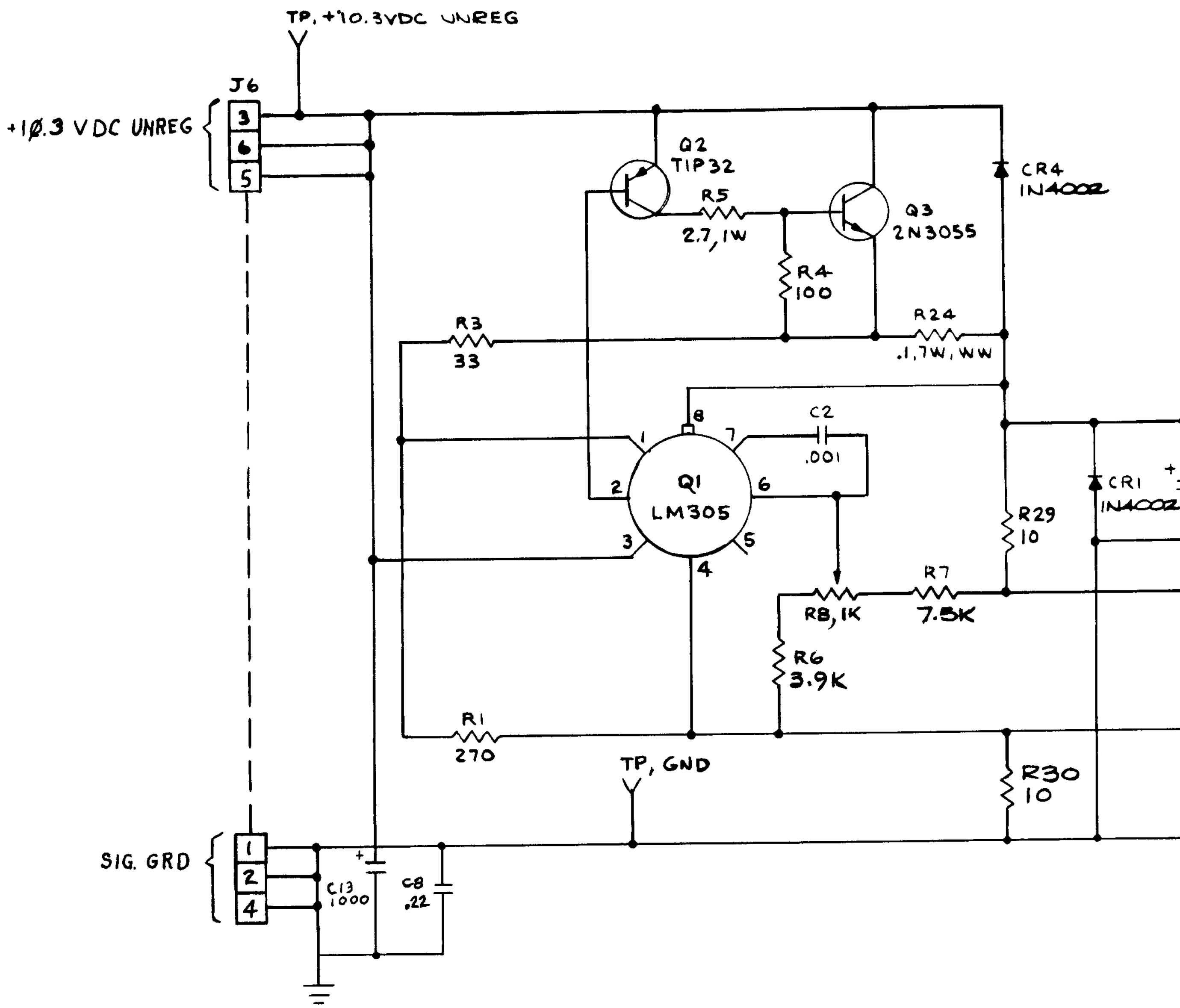
LAST DES	NOT USED
C31	C3-7, 9-12, 14-17, 25-30
CR8	CR2,3
Q11	Q10, 11, 4, 6
R33	R2, 9-23, 26-28

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Kangaroo Reg./Audio II PCB Schematic Diagram

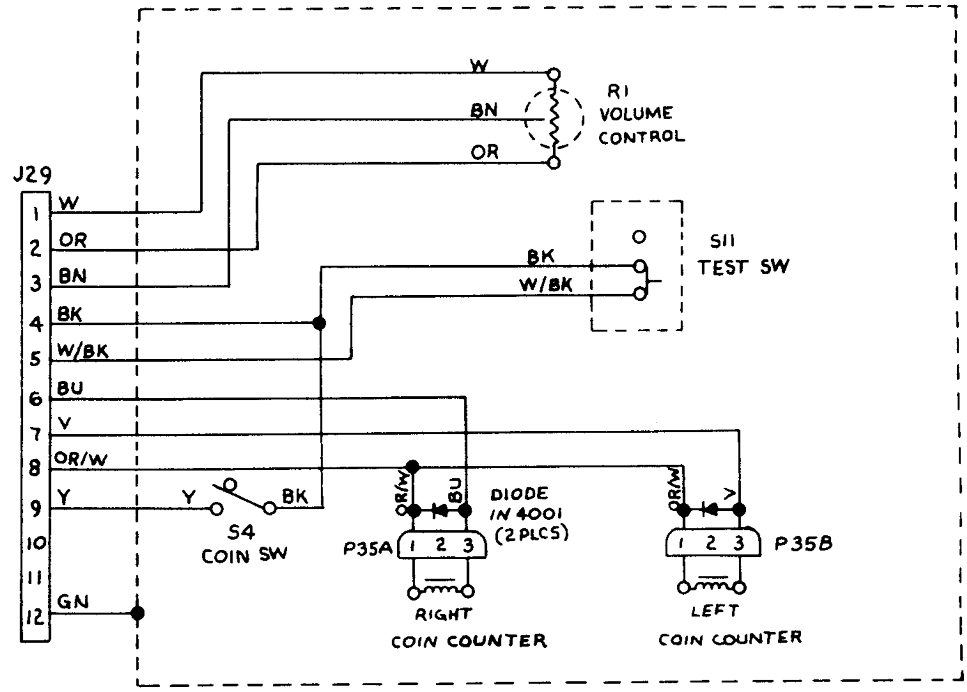
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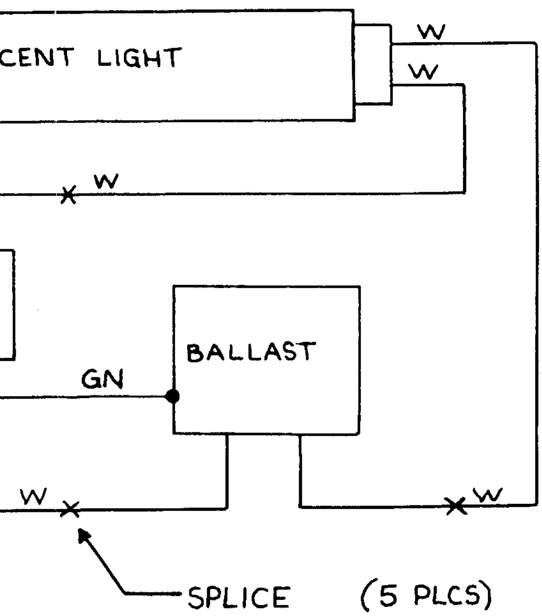


TP, +10.3VDC UNREG
J6
+10.3 VDC UNREG
3
6
5
Q2
TIP32
R5
2.7, 1W
Q3
2N3055
CR4
1N4002
R4
100
R3
33
R24
.1, 7W, WW
8
7
C2
.001
1
2
Q1
LM305
6
3
5
4
CR1
1N4002
R29
10
R7
7.5K
R8, 1K
R6
3.9K
R1
270
TP, GND
R30
10
SIG. GRD
1
2
4
C13
1000
C8
.22

Utility Panel Wiring Diagram



Speaker Wiring Diagram



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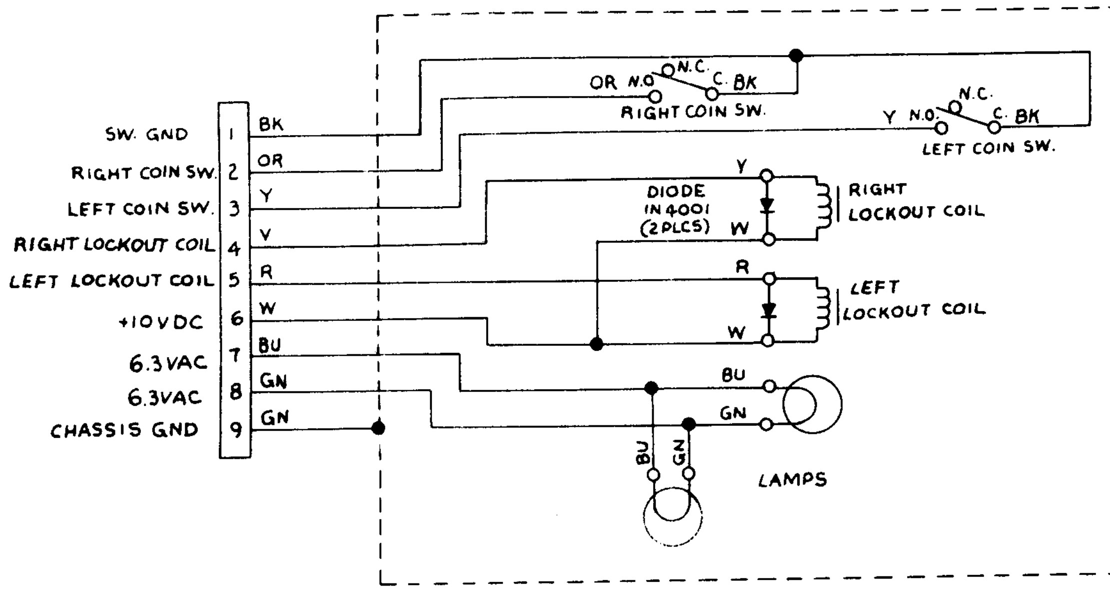
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Kangaroo Game Wiring Interfaces

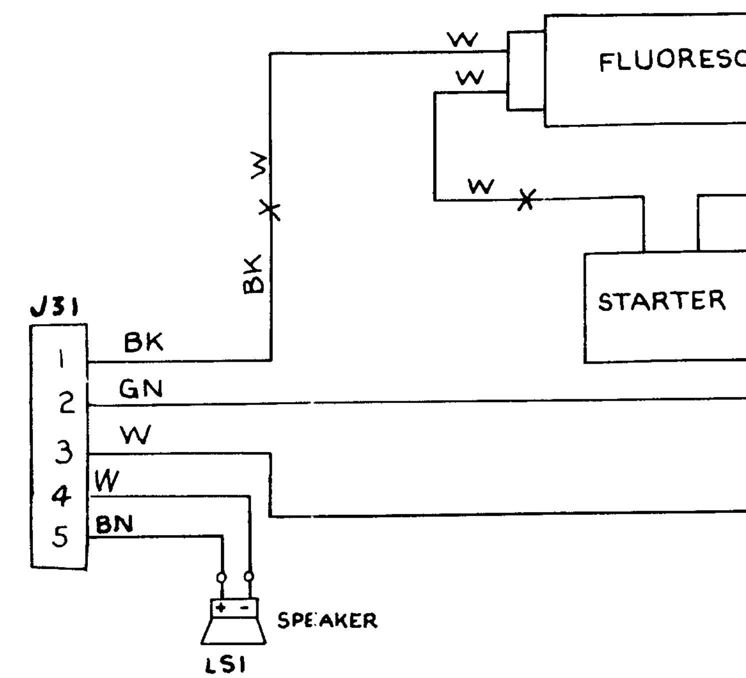
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SP-204 Sheet 3B
3rd printing

Coin Door Wiring Diagram

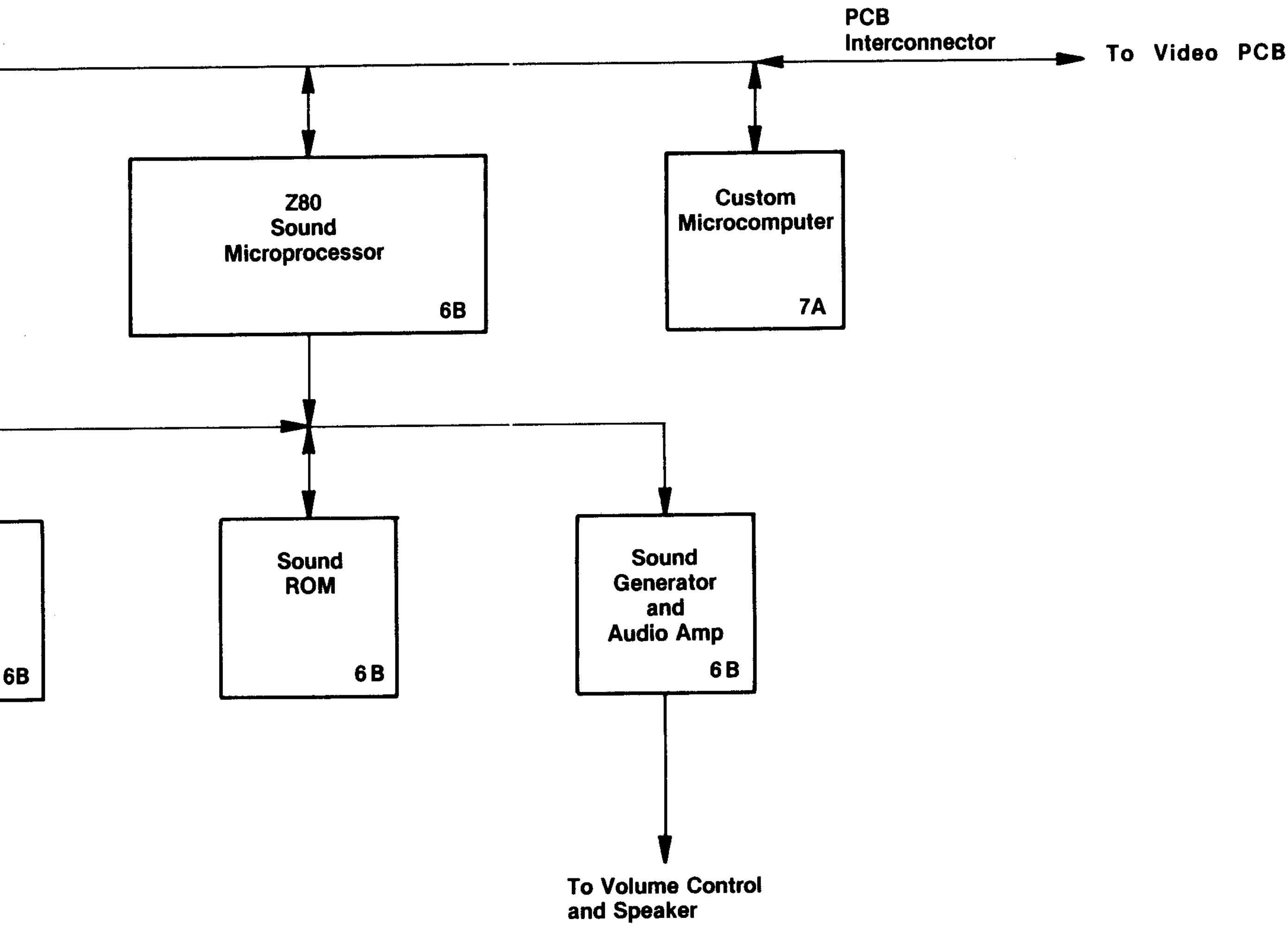


Fluorescent Light and



NOTE

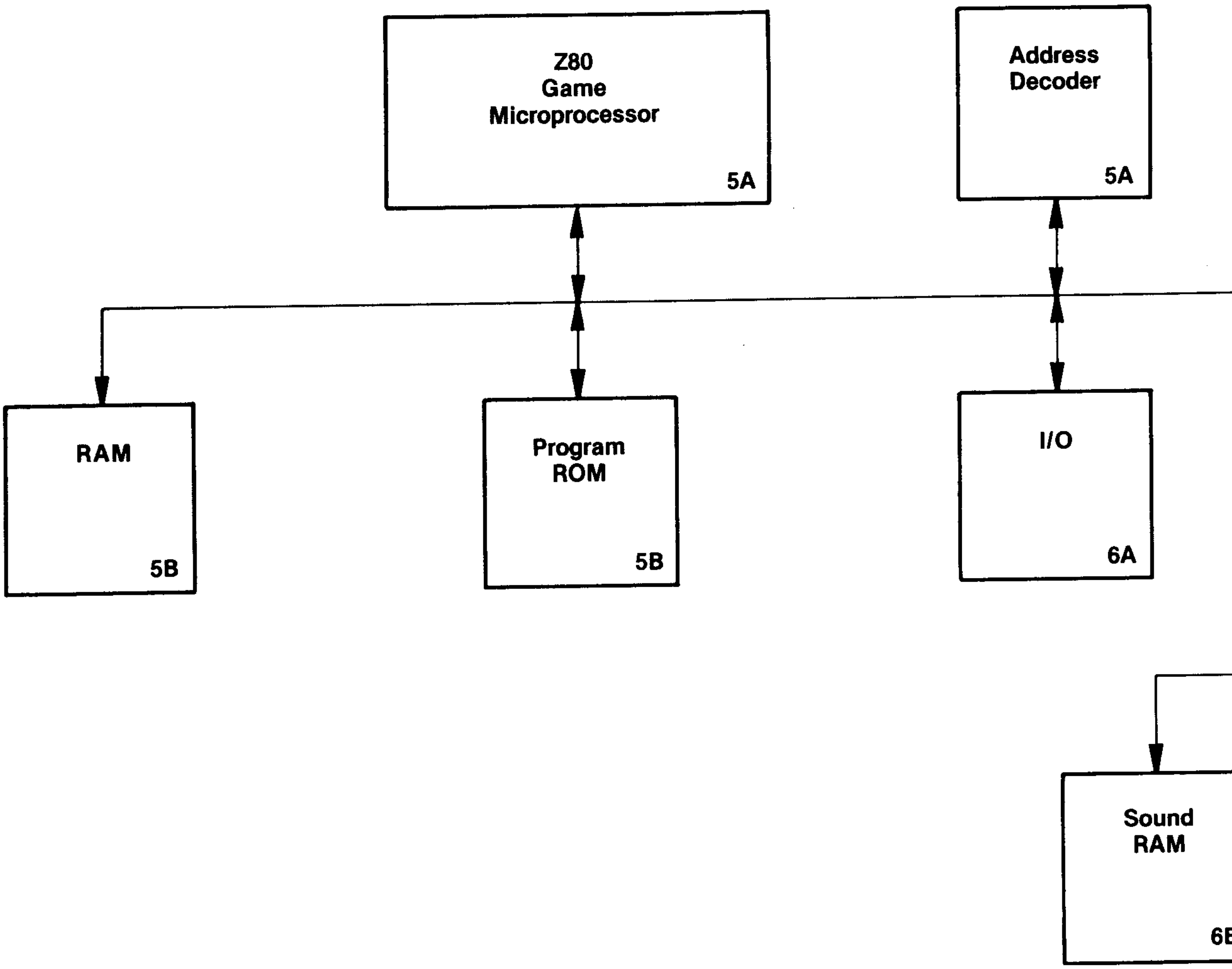
The **service switch**, located on the CPU PCB, allows you to enter credits without tripping the coin counter.



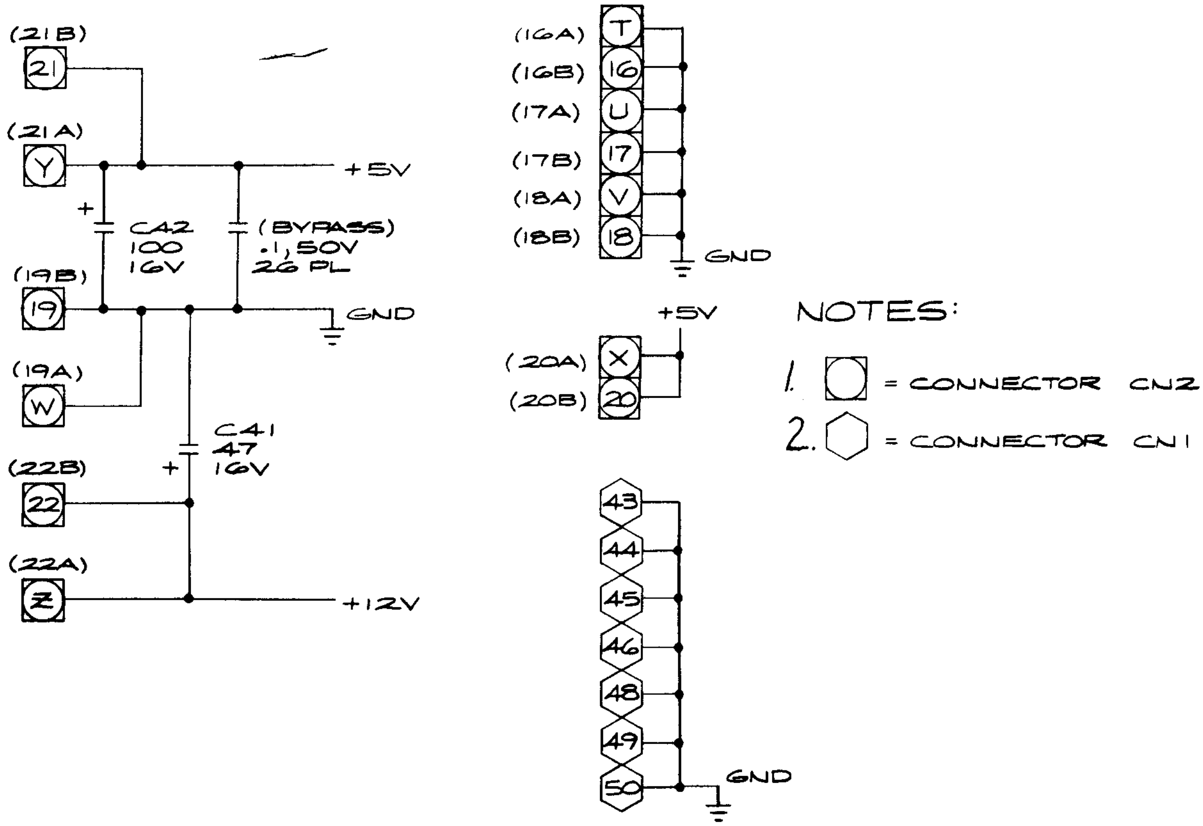
Kangaroo CPU PCB Schematic Diagram

SP-204 Sheet 4A
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Block Diagram (CPU PCB)



CPU Power Input



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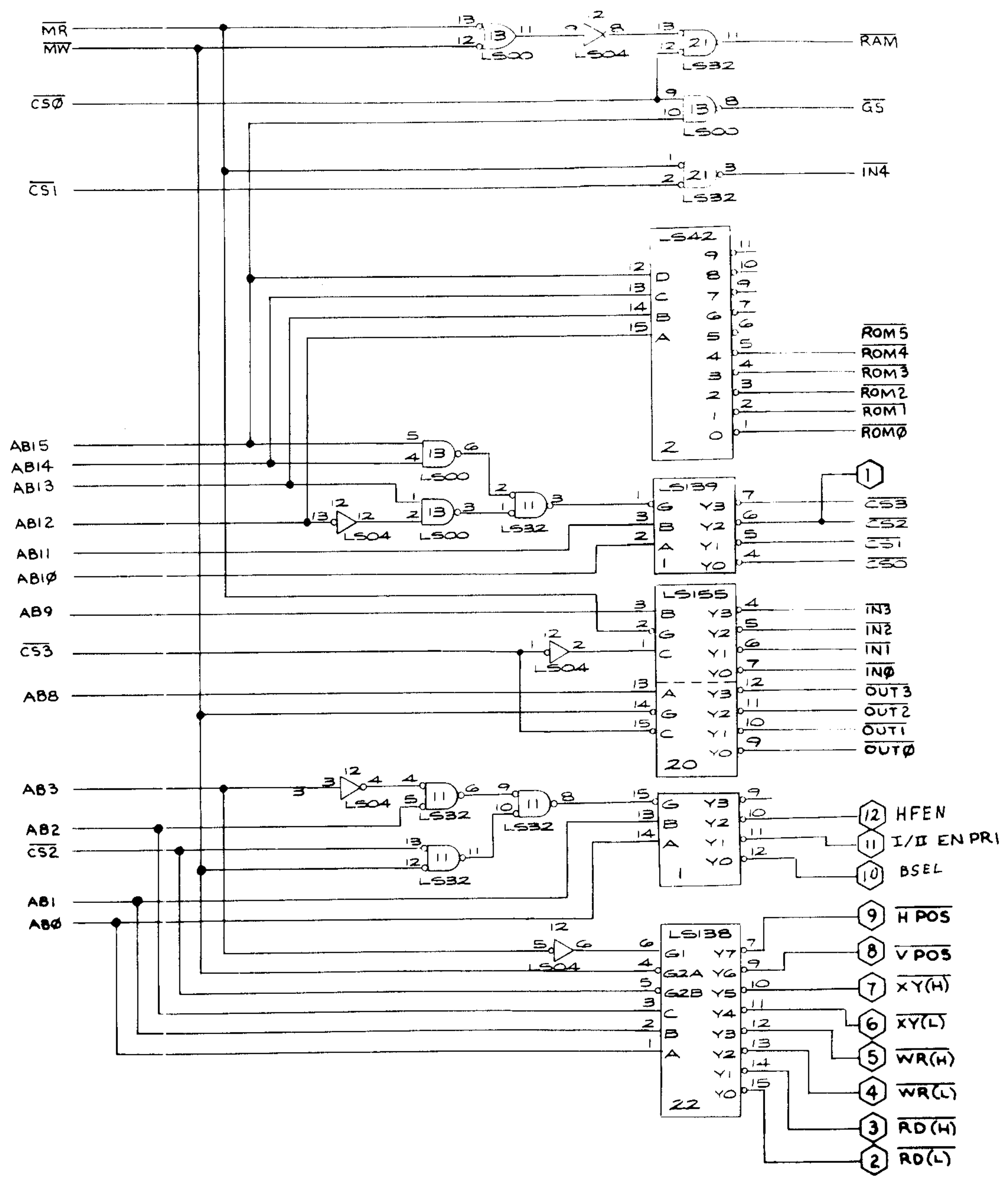
Kangaroo CPU PCB Schematic Diagram

SP-204 Sheet 4B
3rd printing

Memory Map

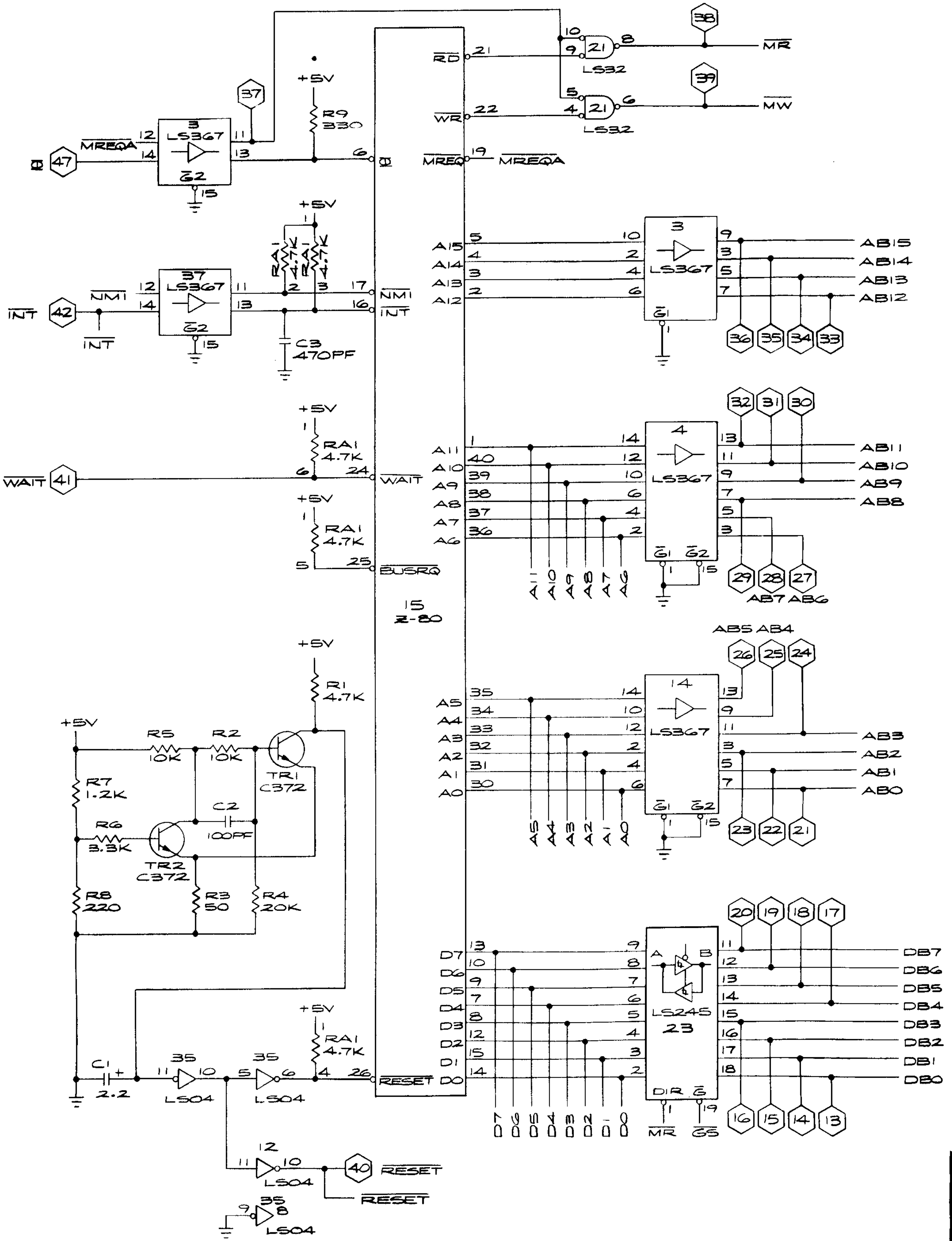
HEXA-DECIMAL ADDRESS	R/W	DATA D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
Game Microprocessor Memory Space (IC15)										
0000-5FFF	R	D	D	D	D	D	D	D	D	Z80 24K Program ROM
E000-E3FF	R/W	D	D	D	D	D	D	D	D	1K Working RAM
E400	R	D	D	D	D	D	D	D	D	Option Switch
E800	W	D	D	D	D	D	D	D	D	Low Byte } Start Address of Data in Picture
E801	W	D	D	D	D	D	D	D	D	High Byte } ROM for DMA
E802	W	D	D	D	D	D	D	D	D	Low Byte } Start Address in Bit Map RAM (where
E803	W	D	D	D	D	D	D	D	D	High Byte } picture is to be written) During DMA
E804	W	D	D	D	D	D	D	D	D	Low Byte } Picture Size for DMA
E805	W	D	D	D	D	D	D	D	D	High Byte } and DMA Start
E806	W	D	D	D	D	D	D	D	D	Vertical Start Address in Bit Map
E807	W	D	D	D	D	D	D	D	D	Horizontal Start Address in Bit Map
E808	W							D	D	Bank Select Latch
E809	W			D	D	D	D	D	D	A & B Bit Map Control Latch (A = playfield, B = motion)
E80A				D	D	D	D	D	D	Color-Shading Latch
EC00	W	D	D	D	D	D	D	D	D	Sound DATA to Sound Microprocessor
EC00	R								D	Utility Coin Switch
EC00	R							D		1 Player Start
EC00	R						D			2 Player Start
EC00	R					D				Left Coin Input
EC00	R				D					Right Coin Input
ED00	W								D	Coin Counter 1
ED00	W							D		Coin Counter 2 (European games)
ED00	R								D	Player 1 Right
ED00	R							D		Player 1 Left
ED00	R						D			Player 1 Up
ED00	R					D				Player 1 Down
ED00	R				D					Player 1 Punch
EE00	R								D	Player 2 Right
EE00	R							D		Player 2 Left
EE00	R						D			Player 2 Up
EE00	R					D				Player 2 Down
EE00	R				D					Player 2 Punch
EFXX	W					D	D	D	D	Output to Custom Microcomputer
EFXX	R					D	D	D	D	Input from Custom Microcomputer
Sound Microprocessor Memory Space (IC34)										
0000-0FFF	R	D	D	D	D	D	D	D	D	4K Program ROM
4000-43FF	R/W	D	D	D	D	D	D	D	D	1K Working RAM
6000	R	D	D	D	D	D	D	D	D	Read DATA from Game Microprocessor
7000	W	D	D	D	D	D	D	D	D	Write to Sound Chip (GI-AY-3-8910)
8000	R	D	D	D	D	D	D	D	D	Read from Sound Chip

Address Decoder



Kangaroo CPU PCB Schematic Diagram

Game Microprocessor



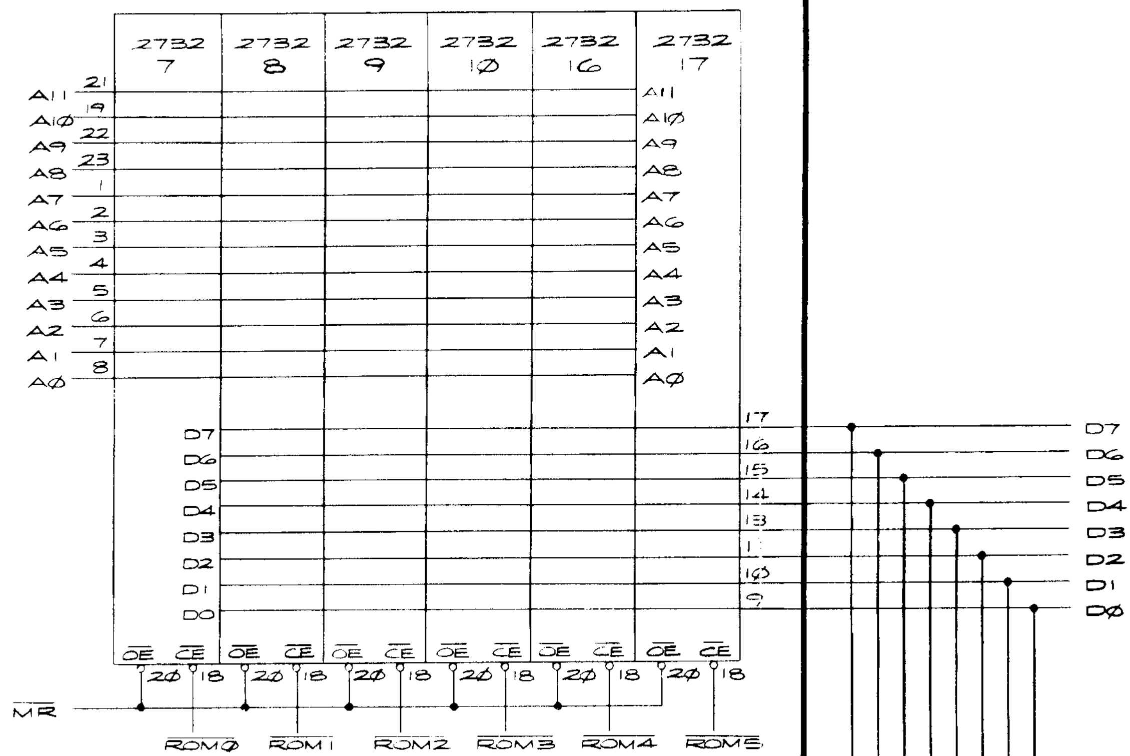
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Kangaroo CPU PCB Schematic Diagram

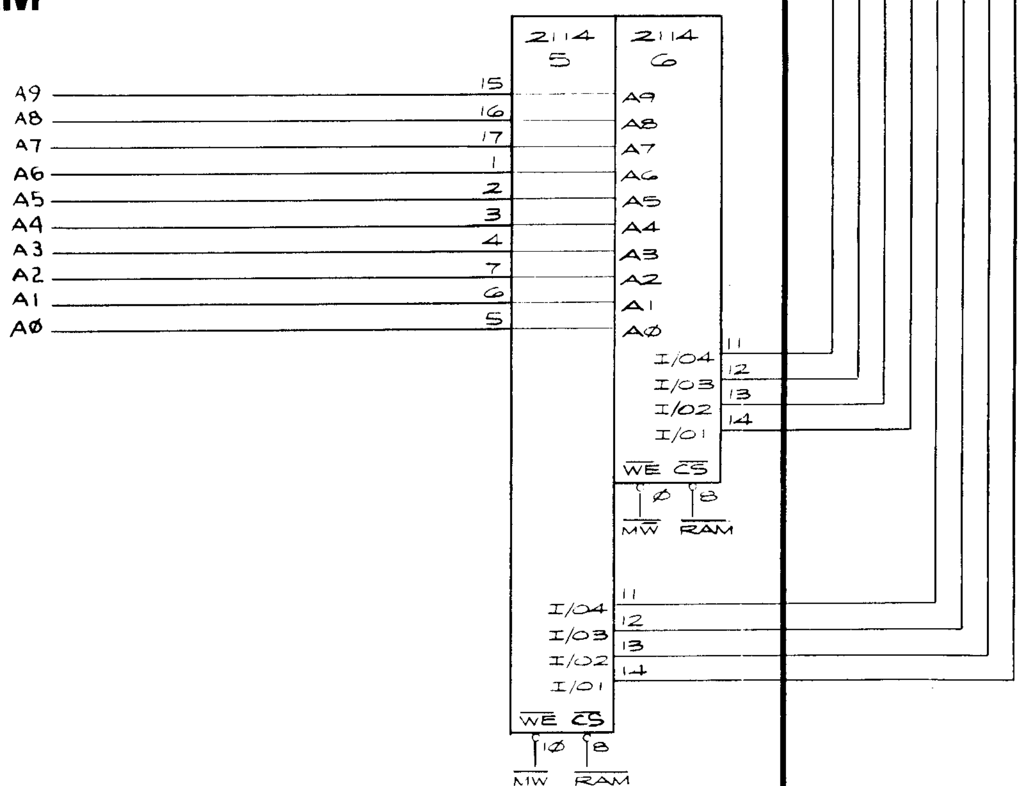
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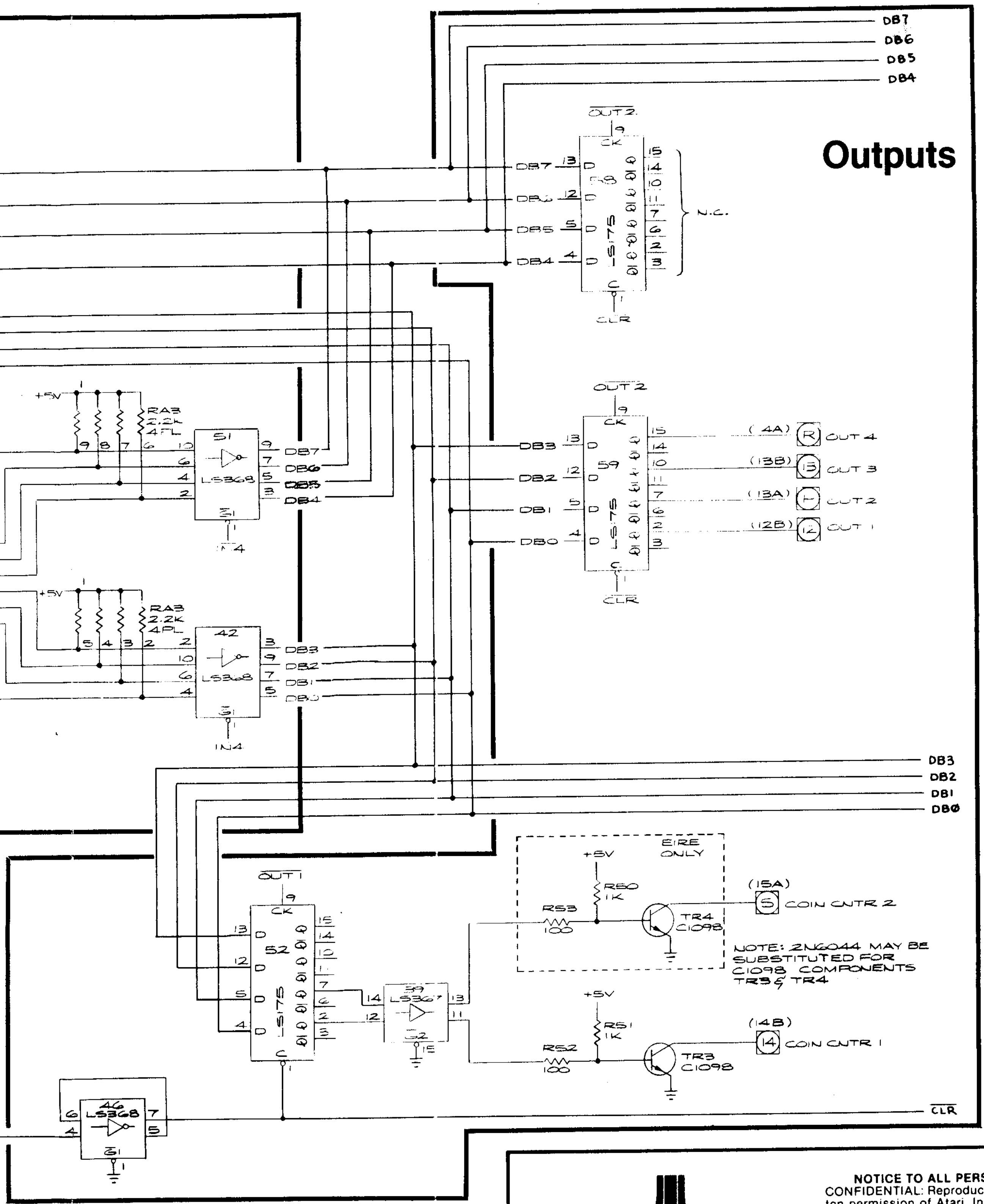
Program ROM



RAM



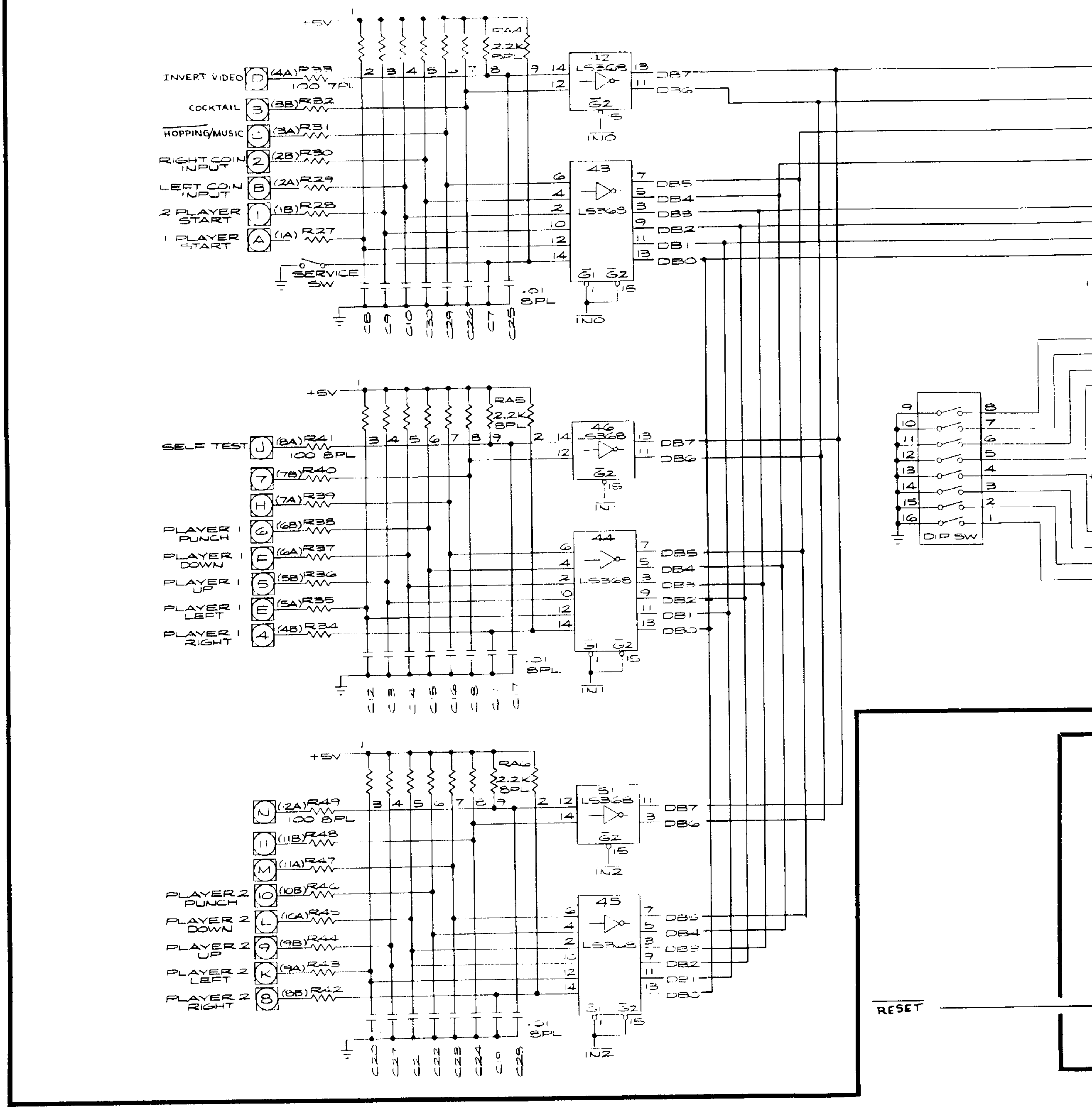
Outputs



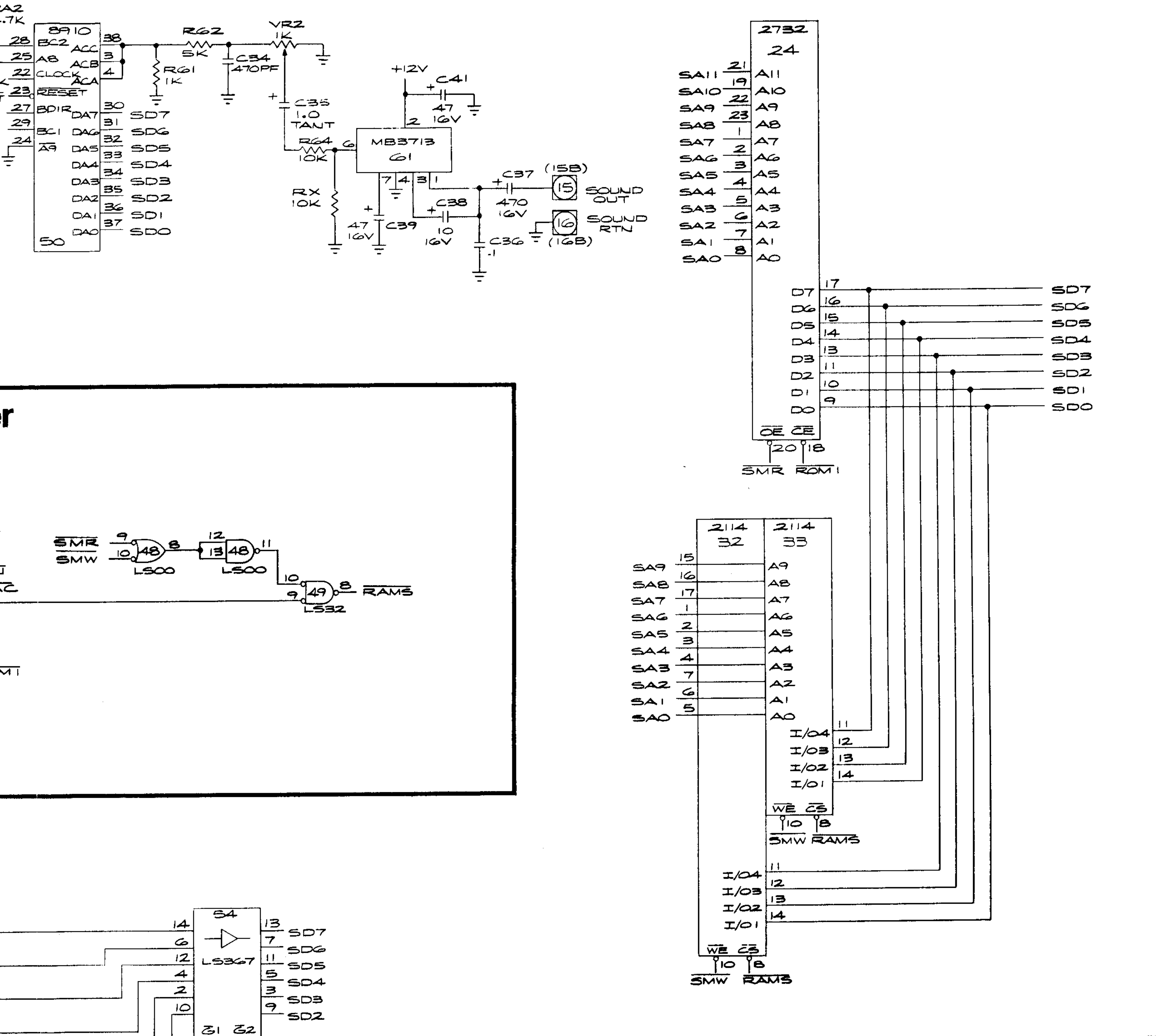
Kangaroo CPU PCB Schematic Diagram

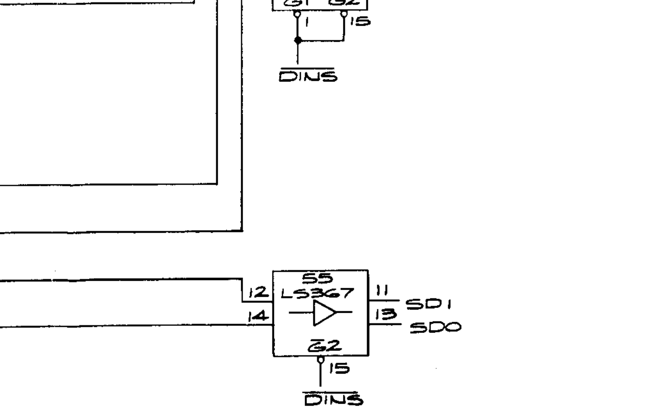
SP-204 Sheet 6A
3rd printing

Inputs



+5V
RA4
2.2K
8PL
INVERT VIDEO
R33
100 7PL
COCKTAIL
R32
HOPPING/MUSIC
R31
RIGHT COIN INPUT
R30
LEFT COIN INPUT
R29
2 PLAYER START
R28
1 PLAYER START
R27
SERVICE SW
.01
8PL
LS368
IN0
DB7
DB6
DB5
DB4
DB3
DB2
DB1
DB0
RA5
SELF TEST
R41
100 8PL
R40
R39
PLAYER 1 PUNCH
R38
PLAYER 1 DOWN
R37
PLAYER 1 UP
R36
PLAYER 1 LEFT
R35
PLAYER 1 RIGHT
R34
IN1
RA6
R49
R48
R47
PLAYER 2 PUNCH
R46
PLAYER 2 DOWN
R45
PLAYER 2 UP
R44
PLAYER 2 LEFT
R43
PLAYER 2 RIGHT
R42
IN2
DIP SW
RESET



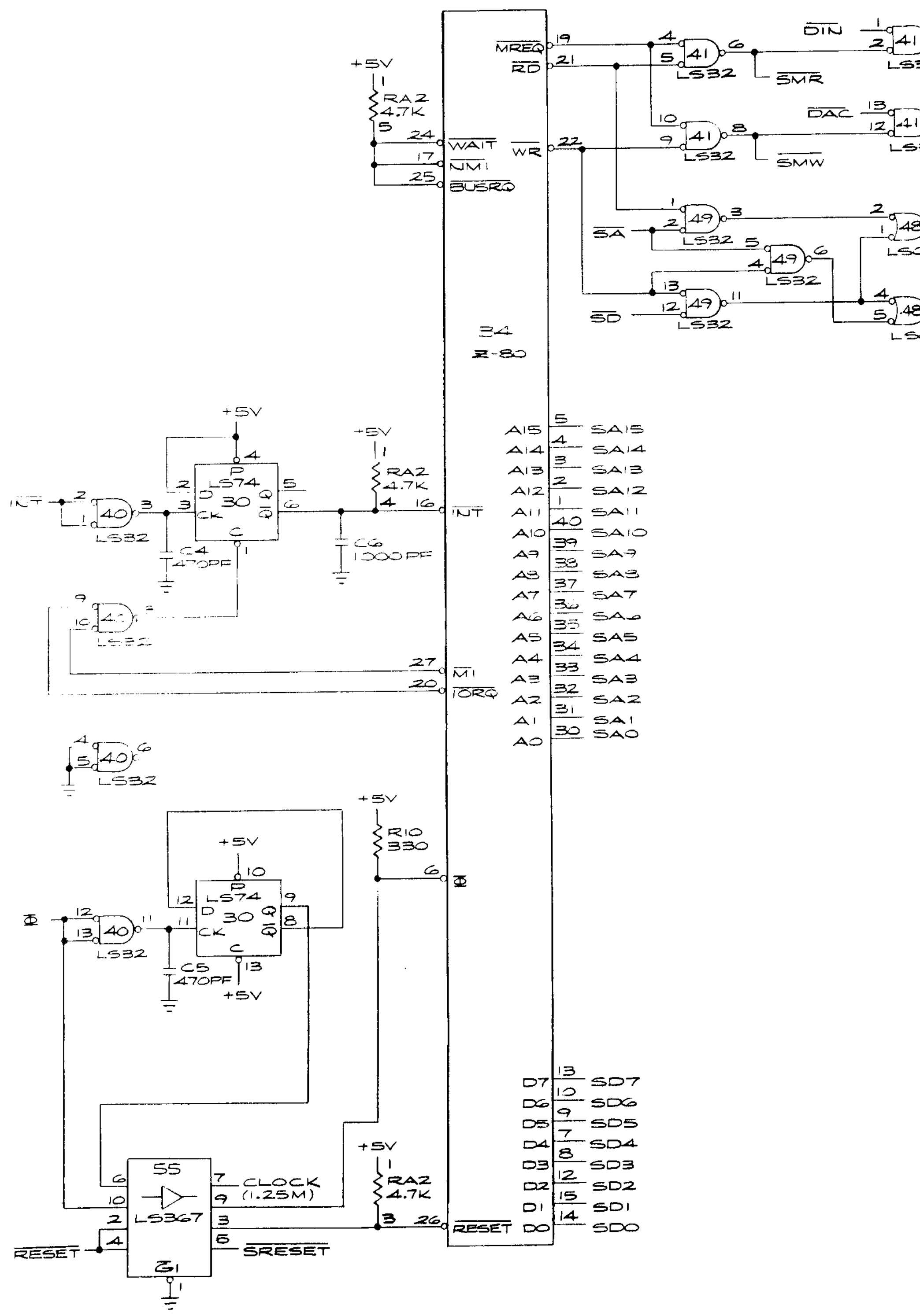


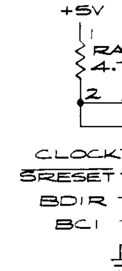
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Kangaroo CPU PCB Schematic Diagram

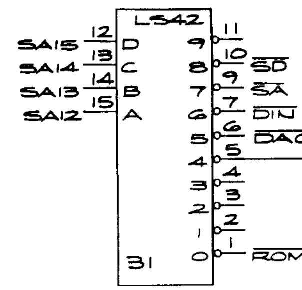
SP-204 Sheet 6B
3rd printing

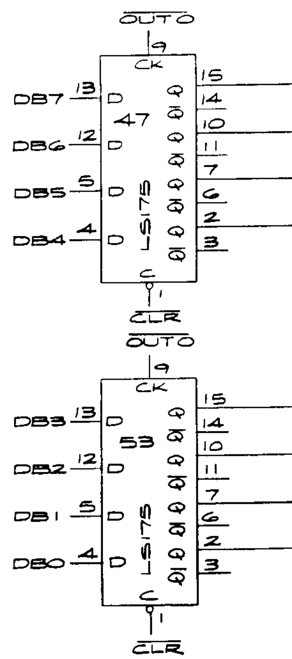
Sound Microprocessor

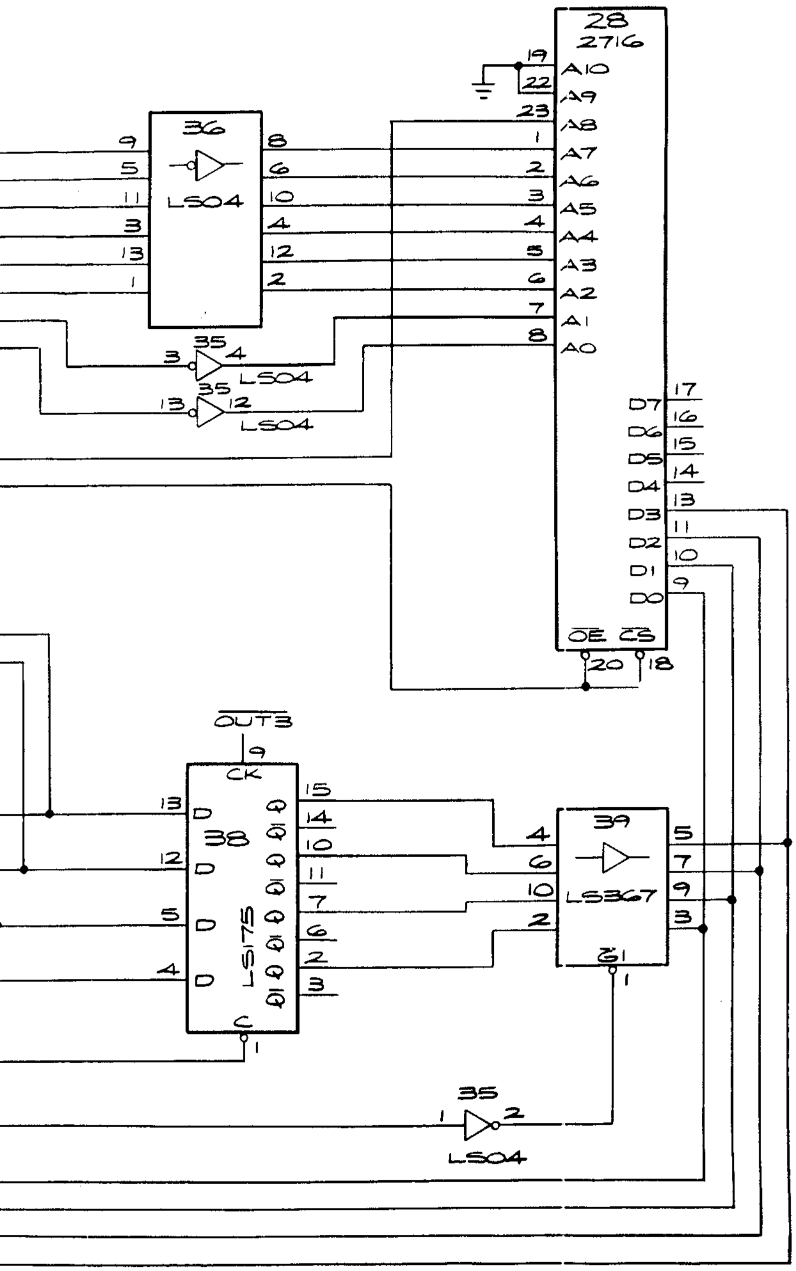




Address Decoder



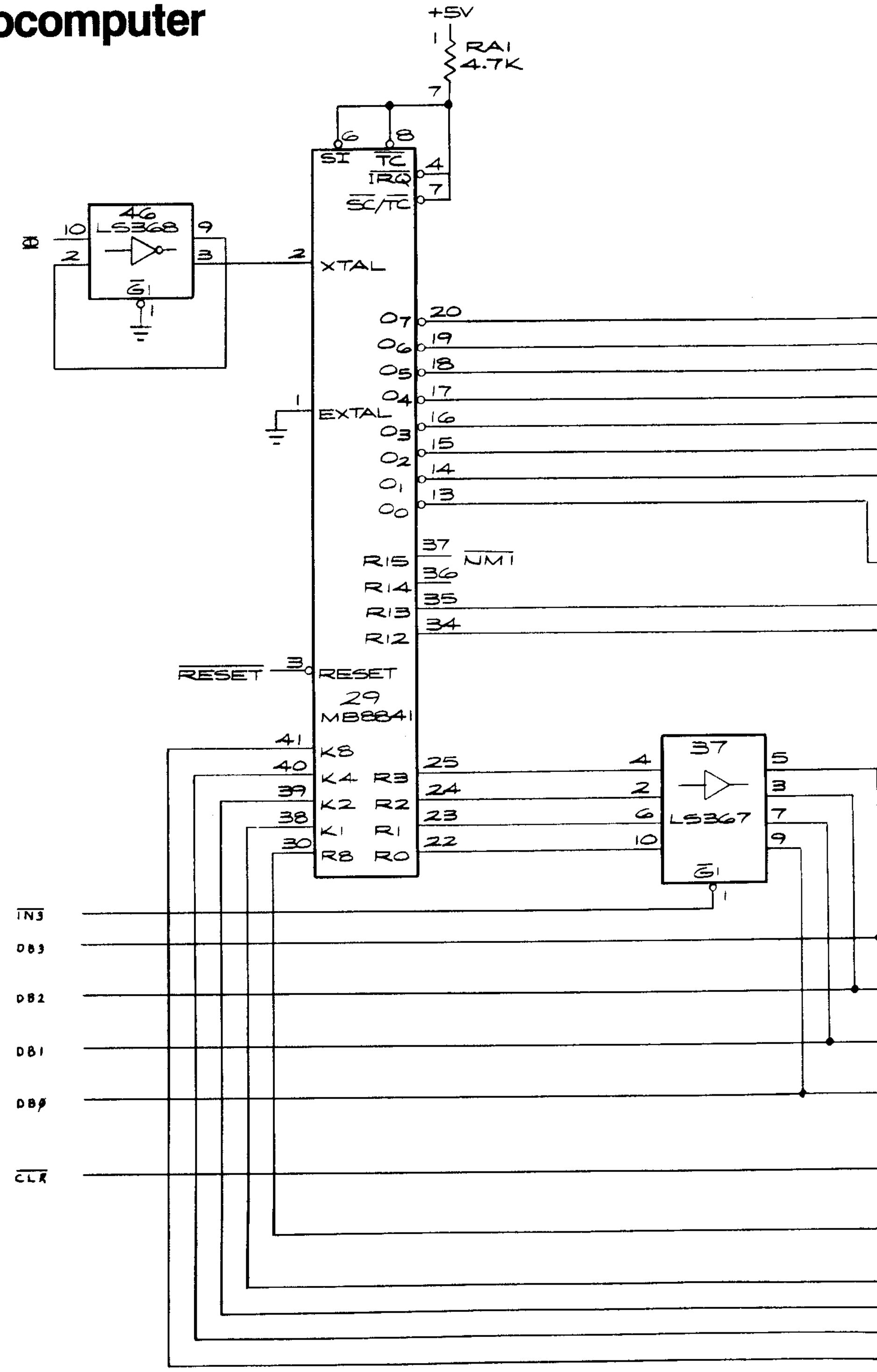


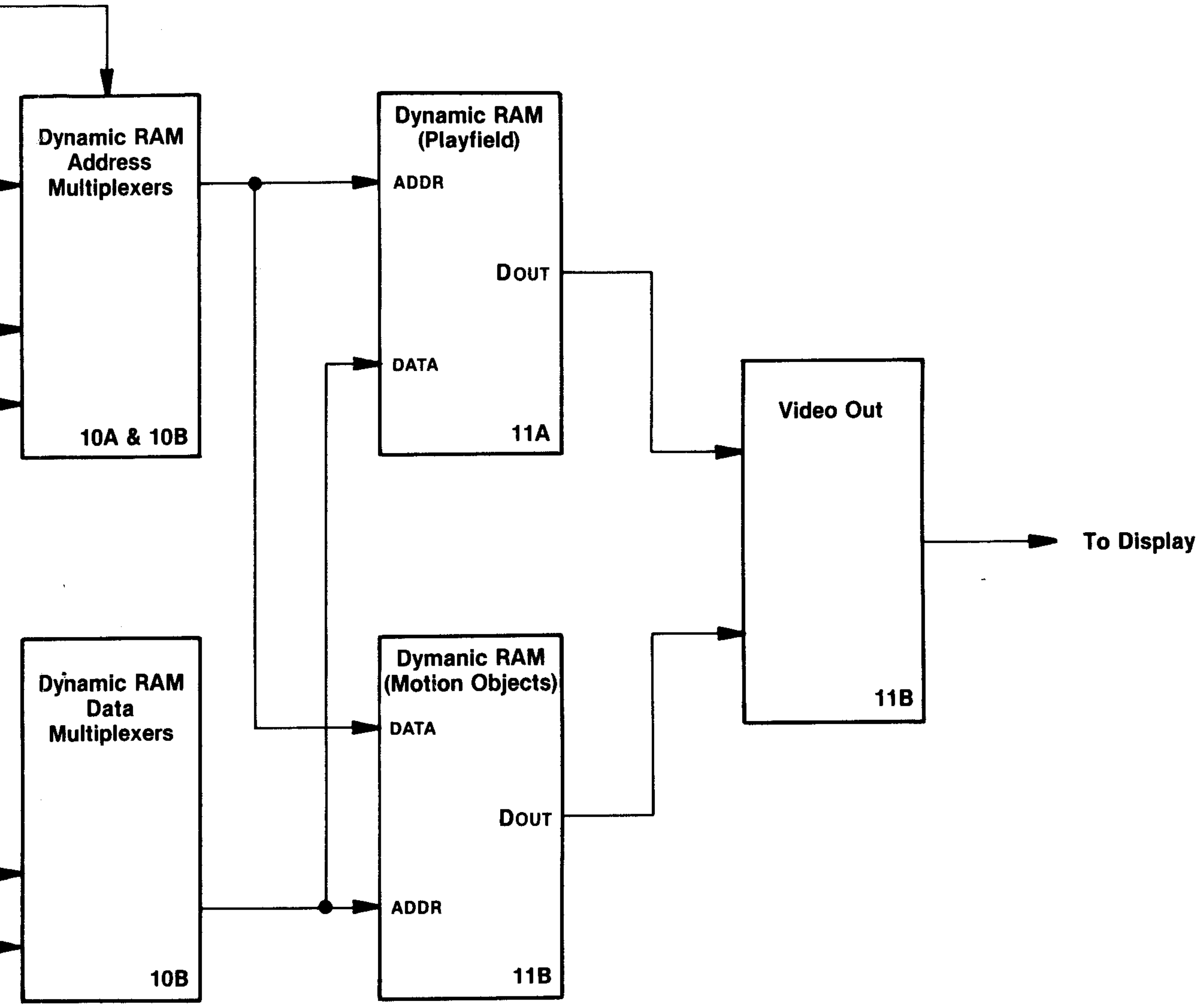


Kangaroo CPU PCB Schematic Diagram

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Custom Microcomputer





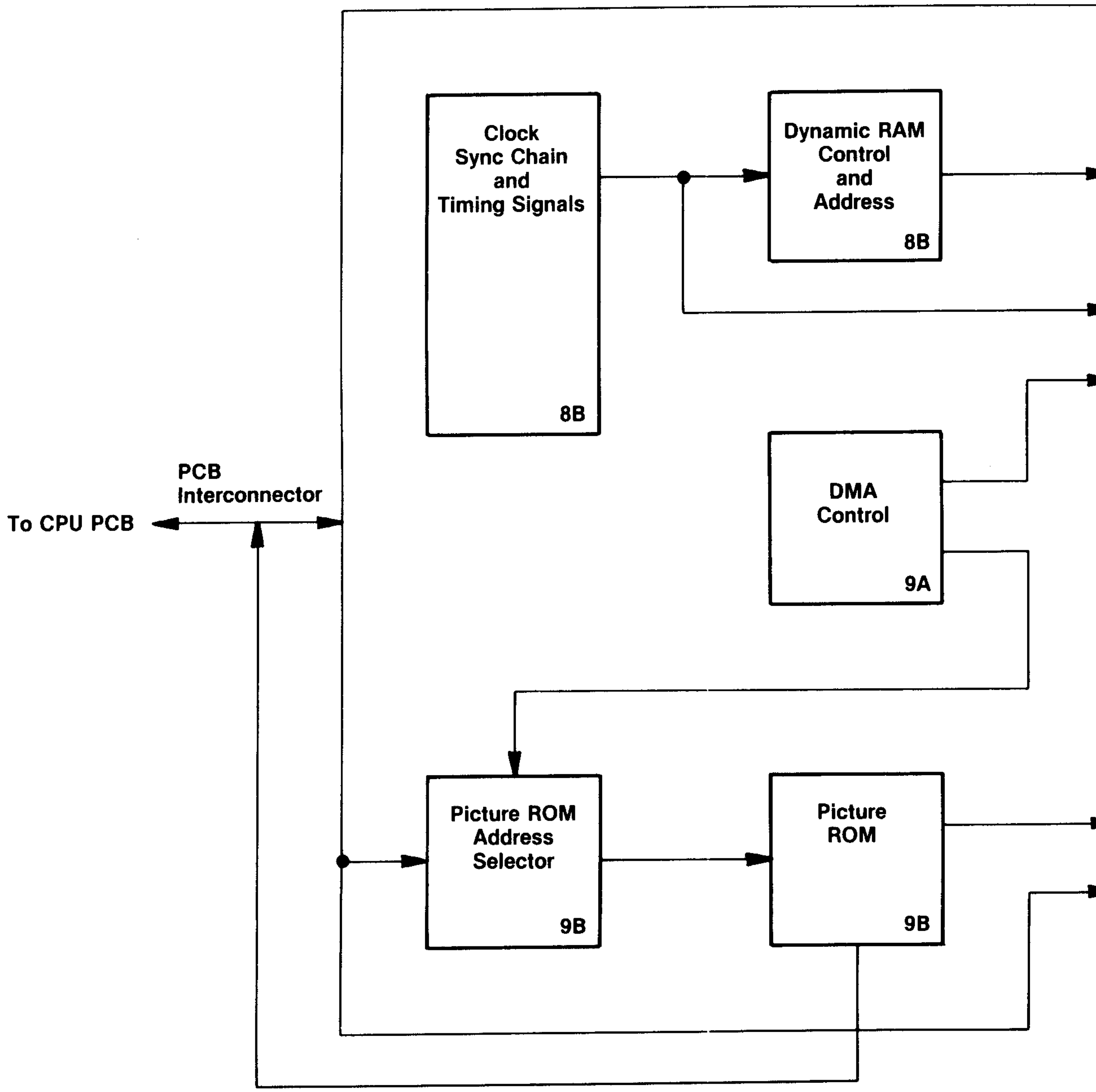
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Kangaroo Video PCB Schematic Diagram

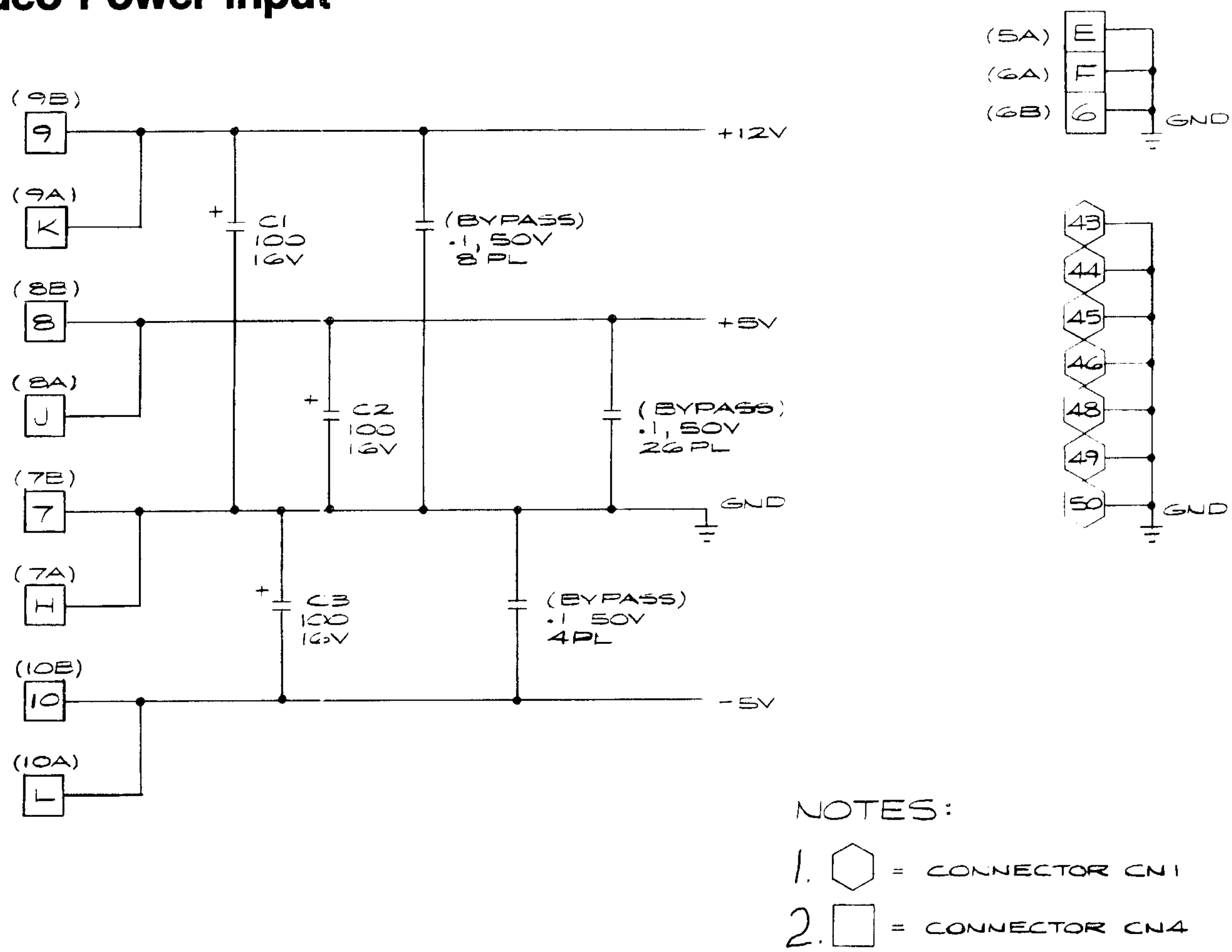
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Block Diagram (Video PCB)



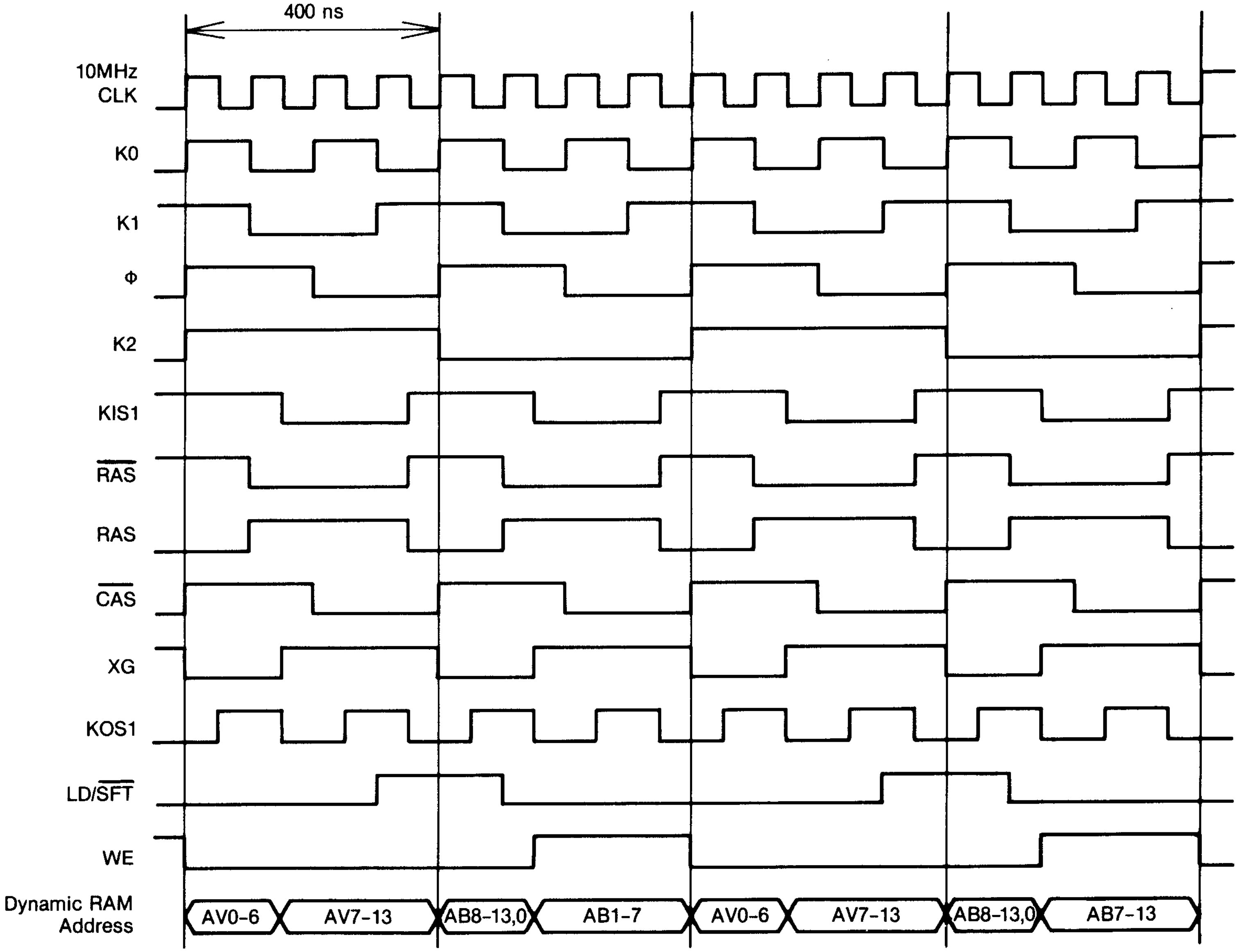
Video Power Input



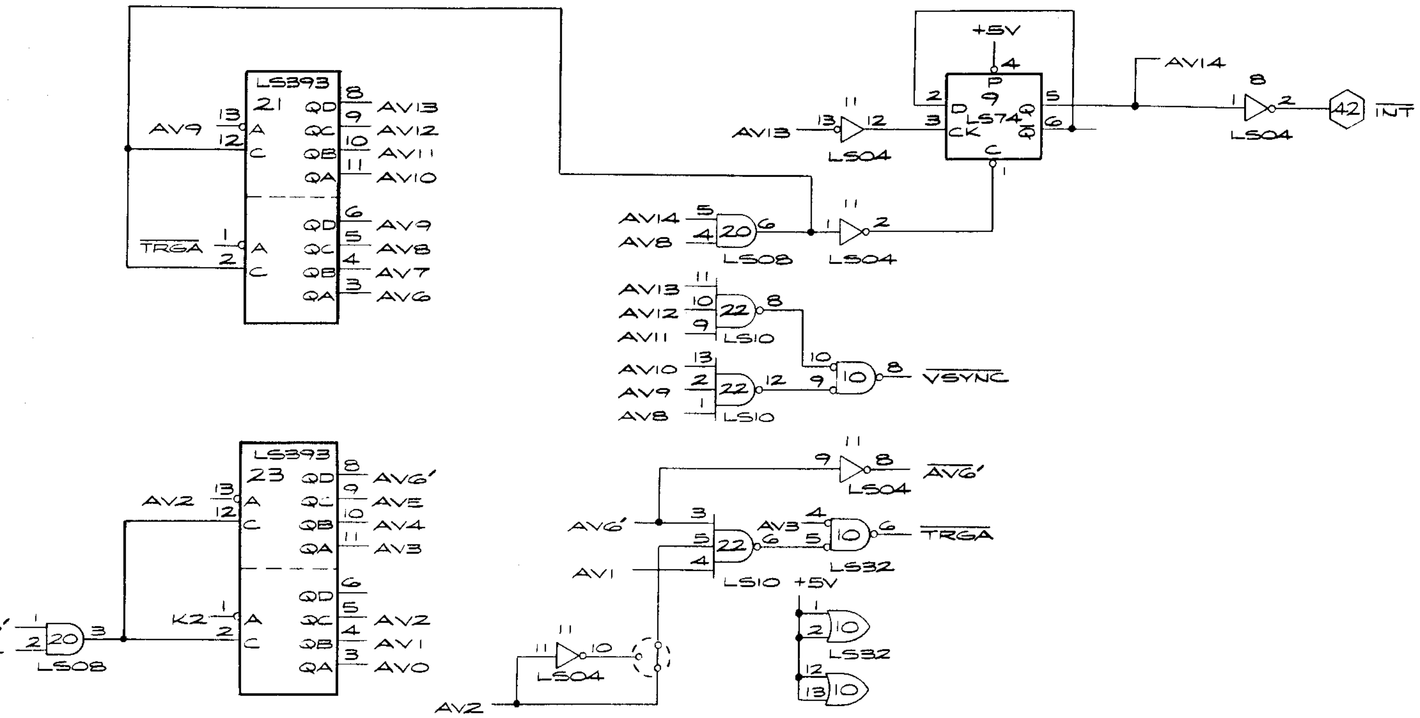
Kangaroo Video PCB Schematic Diagram

SP-204 Sheet 8A
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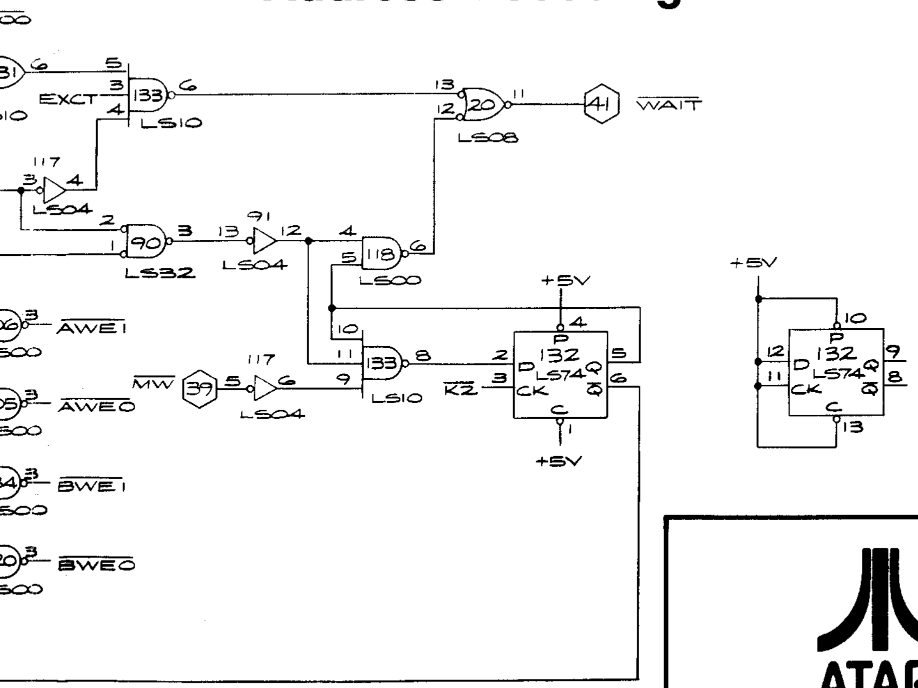
Dynamic RAM Timing Diagram (Video PCB)



nd Timing Signals



Address Decoding



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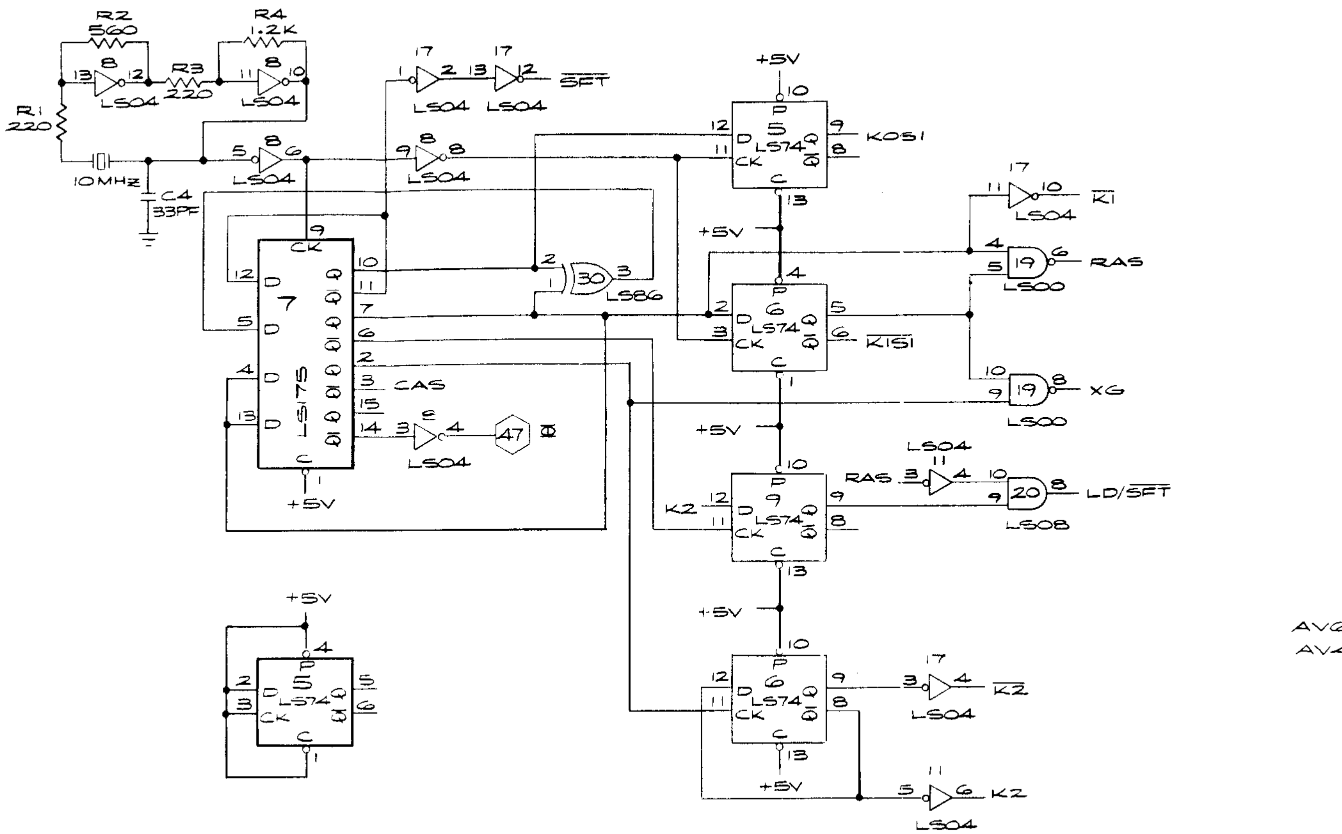
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Kangaroo Video PCB Schematic Diagram

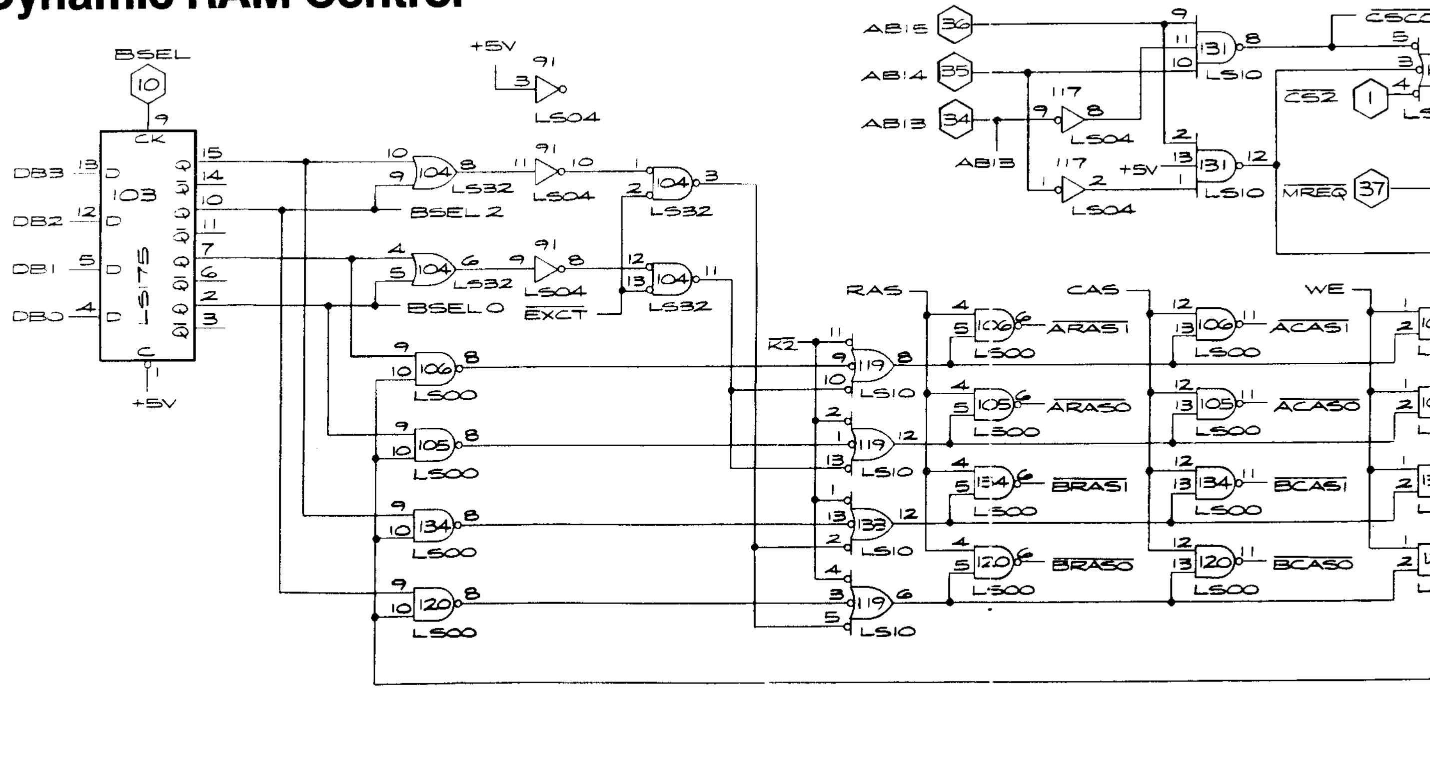
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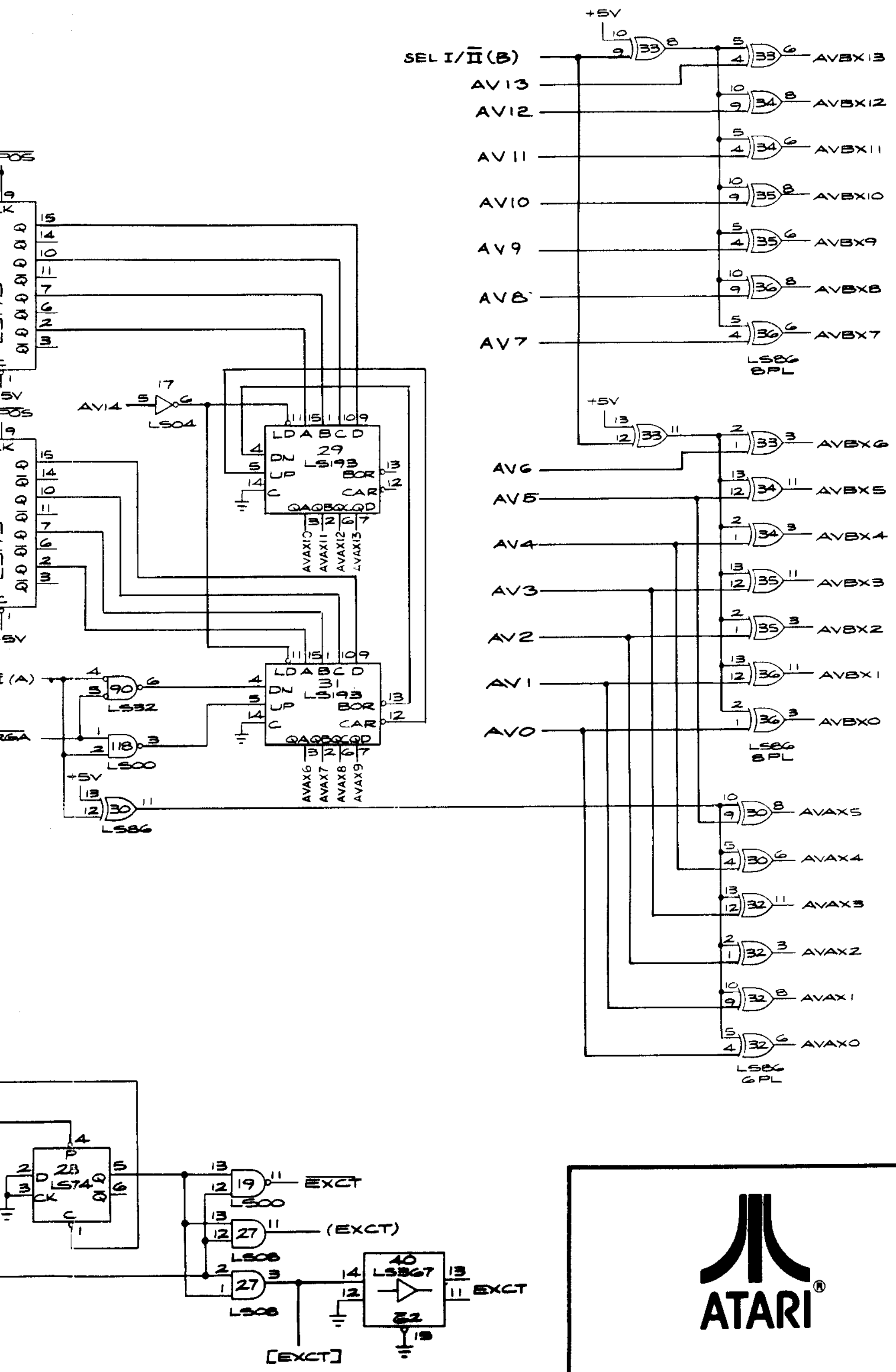
Clock, Sync Chain, a



Dynamic RAM Control



Dynamic RAM Video Address and Flip



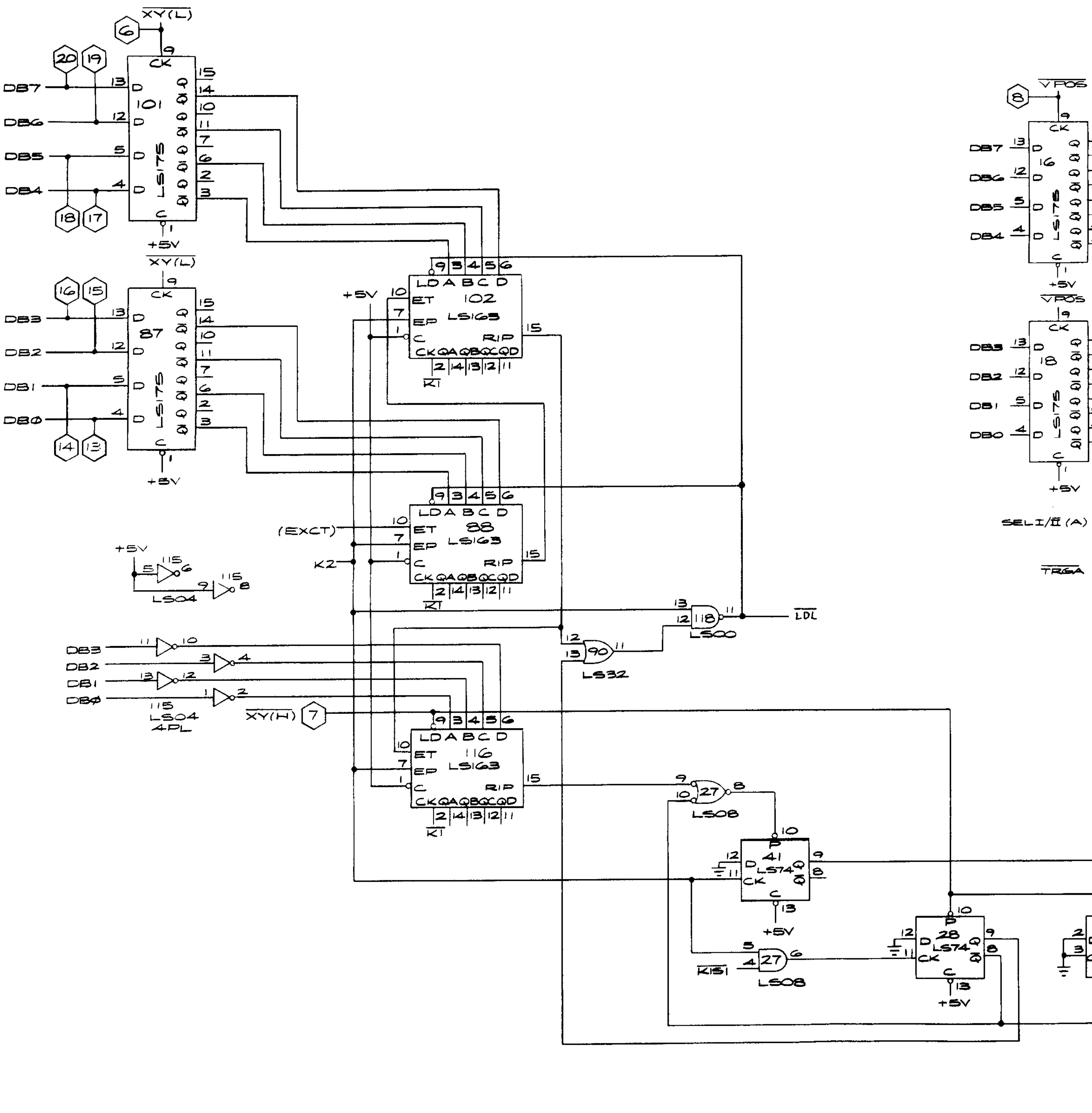
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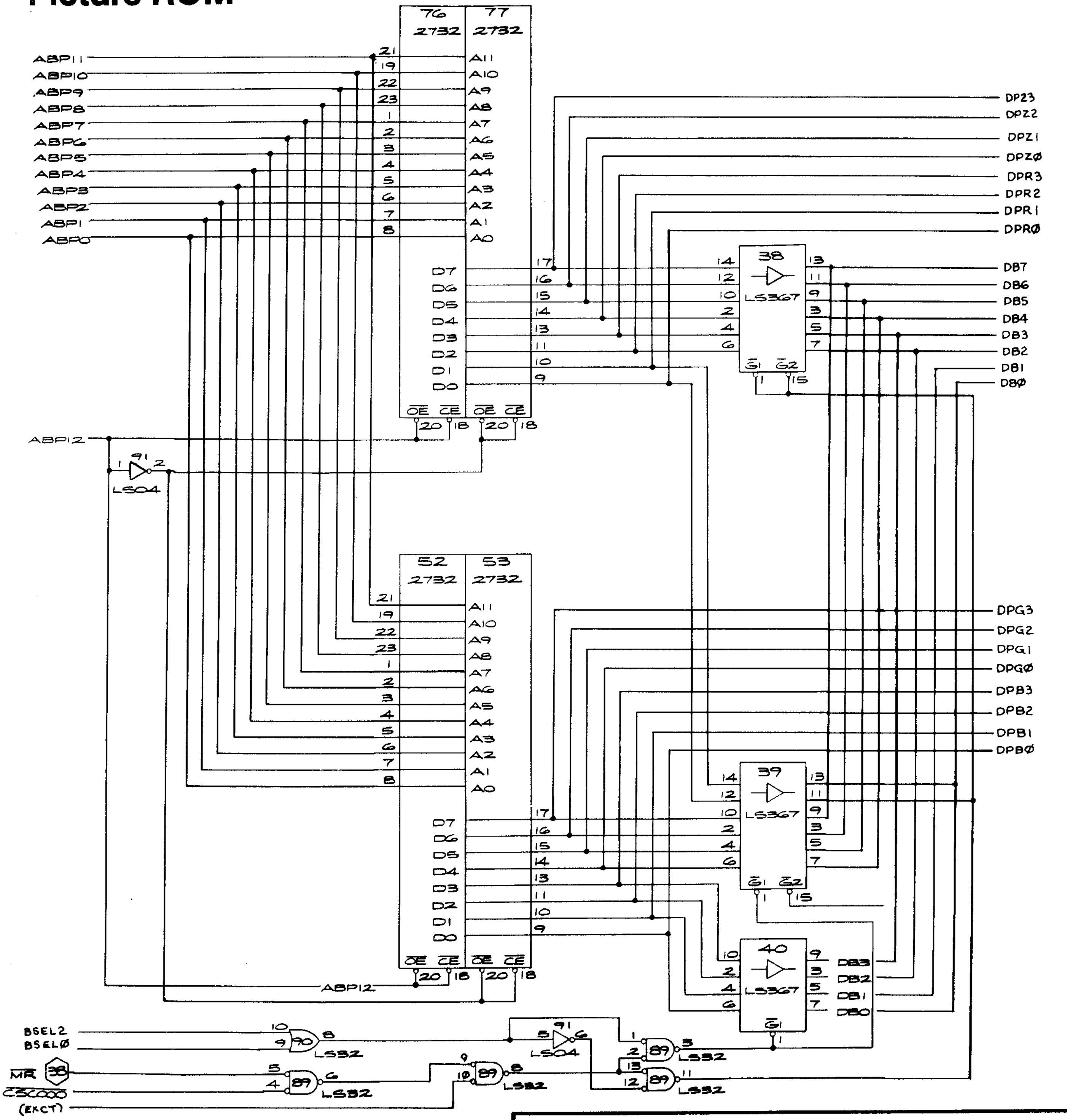
Kangaroo Video PCB Schematic Diagram

SP-204 Sheet 9A
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DMA Control


XY(L)
DB7
DB6
DB5
DB4
101
LS175
+5V
XY(L)
DB3
DB2
DB1
DBØ
87
LS175
+5V
102
LS163
+5V
88
LS163
(EXCT)
K2
116
LS163
LS04
LS04
4PL
XY(H)
118
LS00
LDL
90
LS32
27
LS08
41
LS74
28
LS74
KIS1
VPOS
16
LS175
18
LS175
SEL I/II (A)
TRGA

Picture ROM



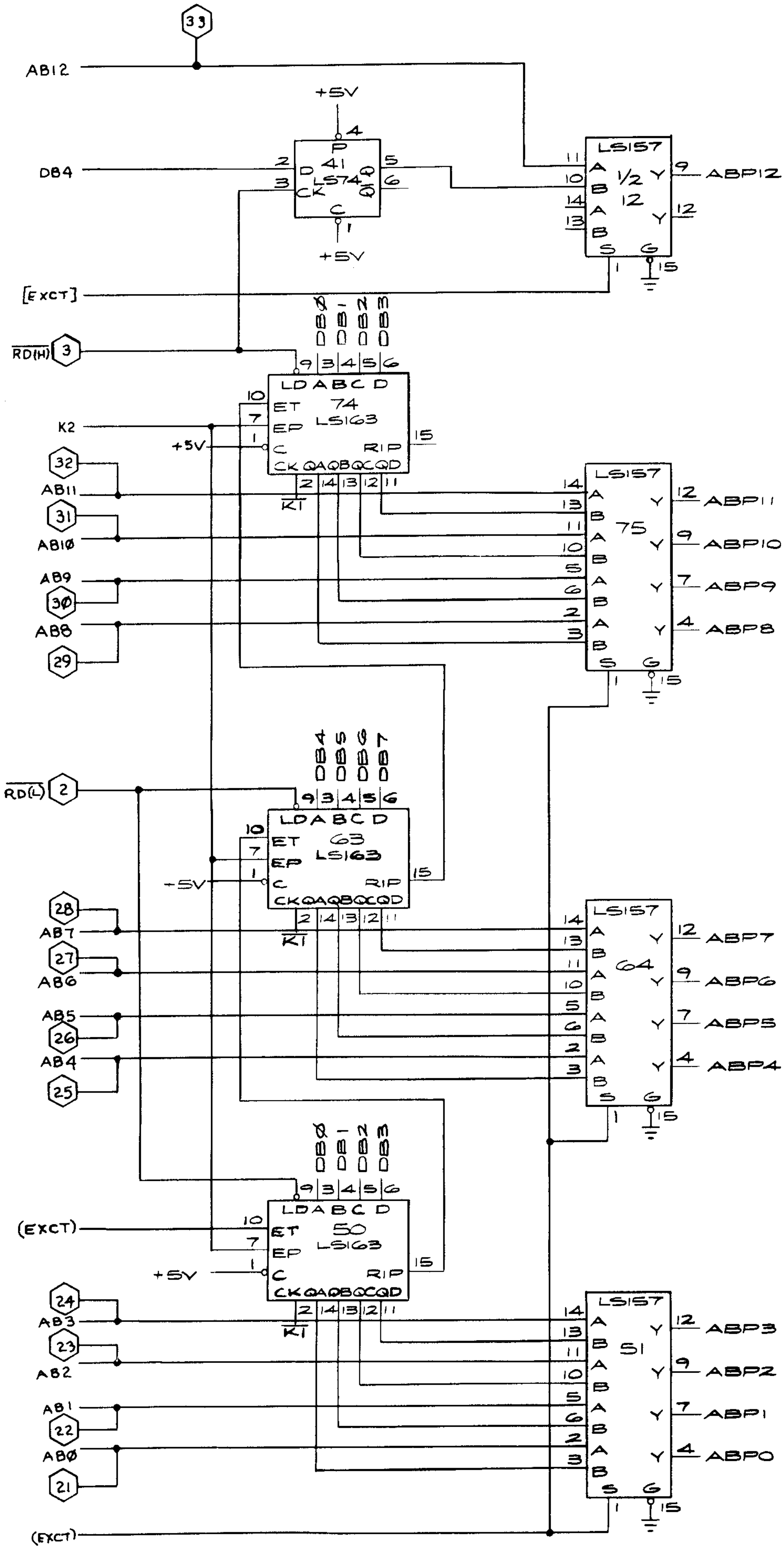
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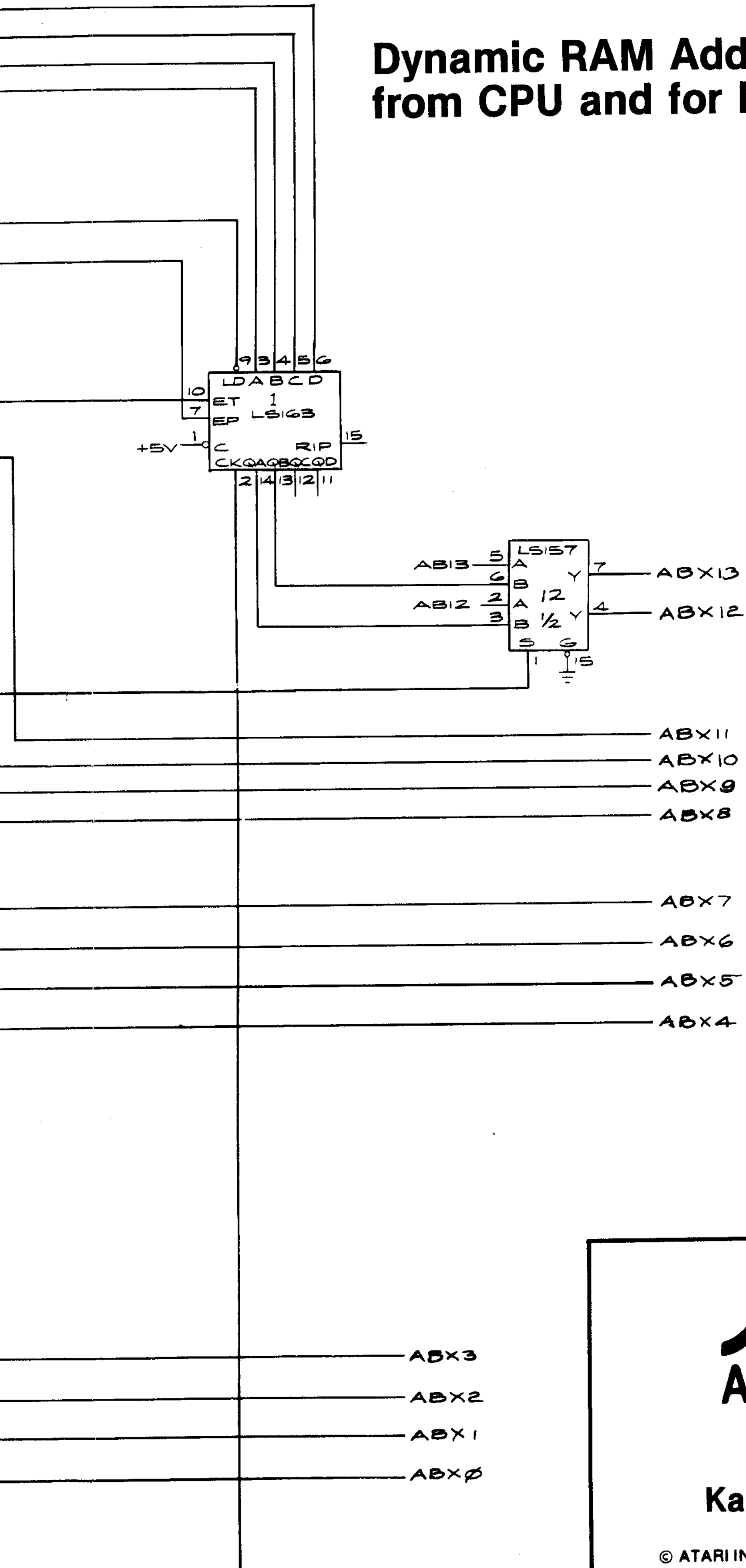
Kangaroo Video PCB Schematic Diagram

SP-204 Sheet 9B
3rd printing

Picture ROM Address Selector



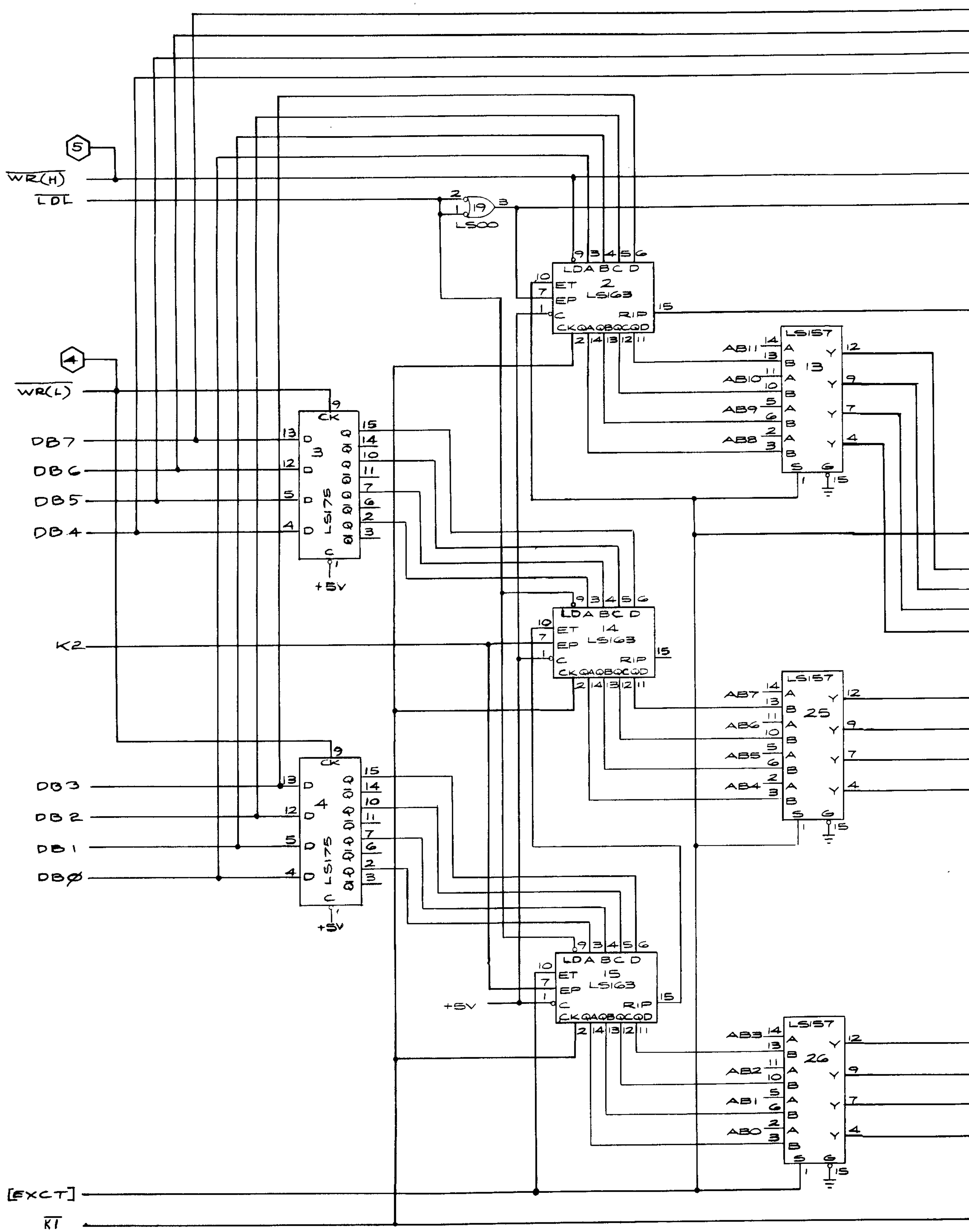
Dynamic RAM Address from CPU and for DMA



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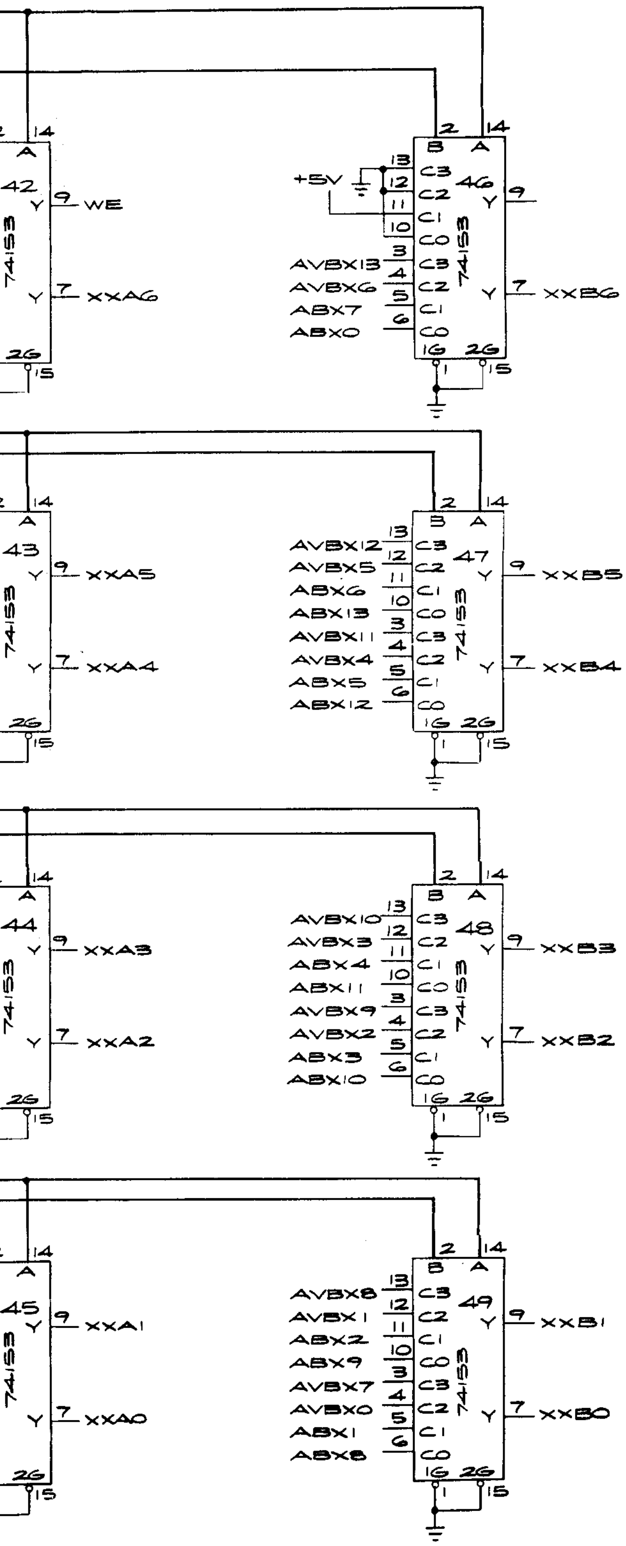
Kangaroo Video PCB Schematic Diagram

SP-204 **Sheet 10A**
3rd printing



5
WR(H)
LDL
19
LS00
2
LS163
4
WR(L)
DB7
DB6
DB5
DB4
3
LS175
+5V
LS157
13
AB11
AB10
AB9
AB8
14
K2
DB3
DB2
DB1
DBØ
4
25
AB7
AB6
AB5
AB4
15
26
AB3
AB2
AB1
AB0
[EXCT]
KI

Address Selector

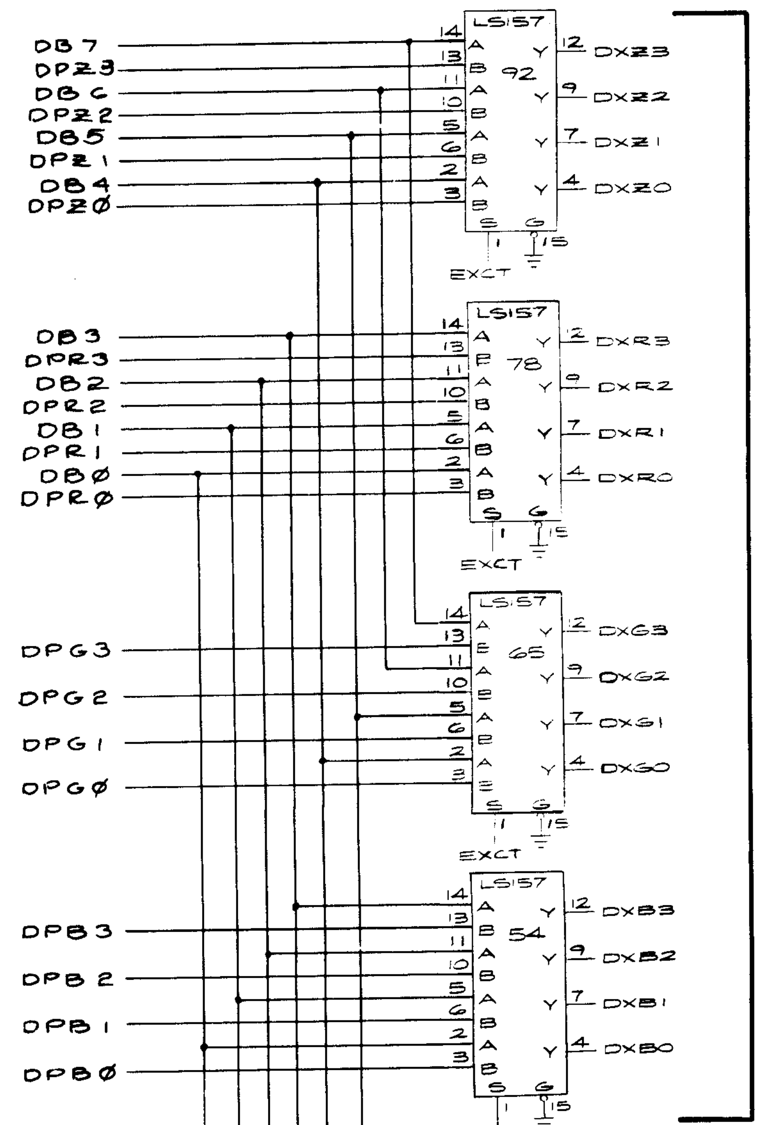


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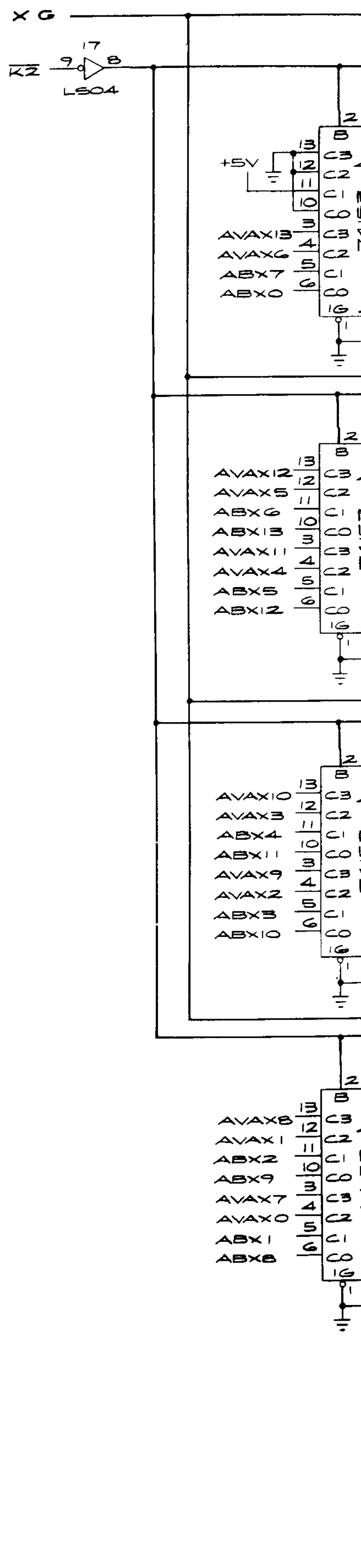
Kangaroo Video PCB Schematic Diagram

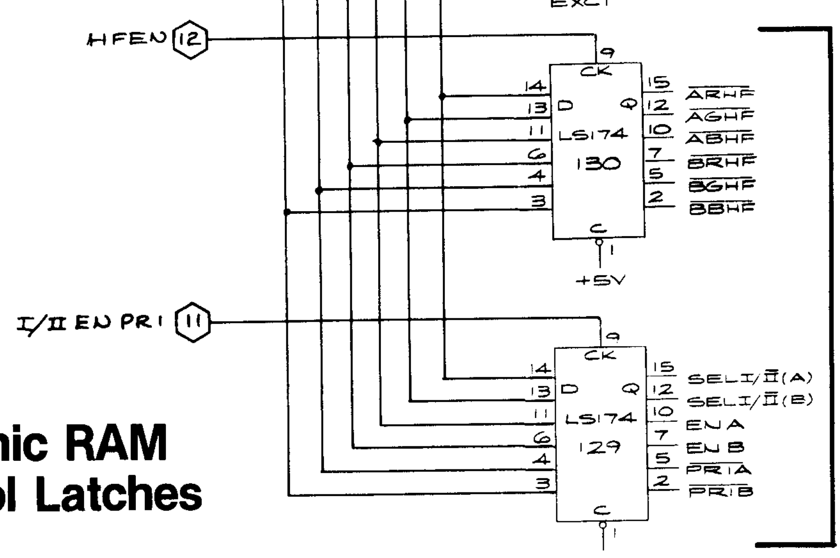
SP-204 Sheet 10B
3rd printing

Dynamic RAM Data Selector



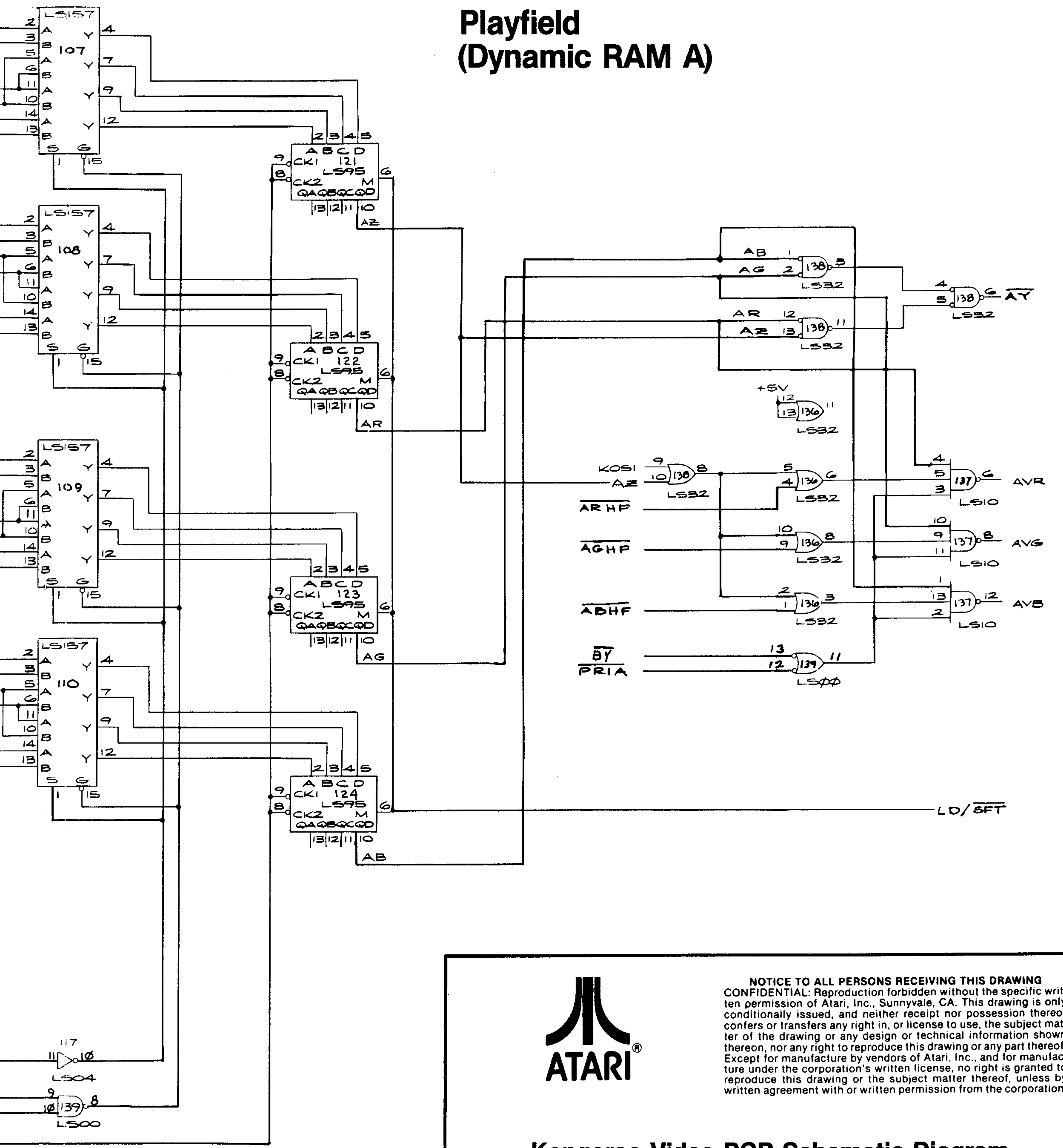
Dynamic RAM





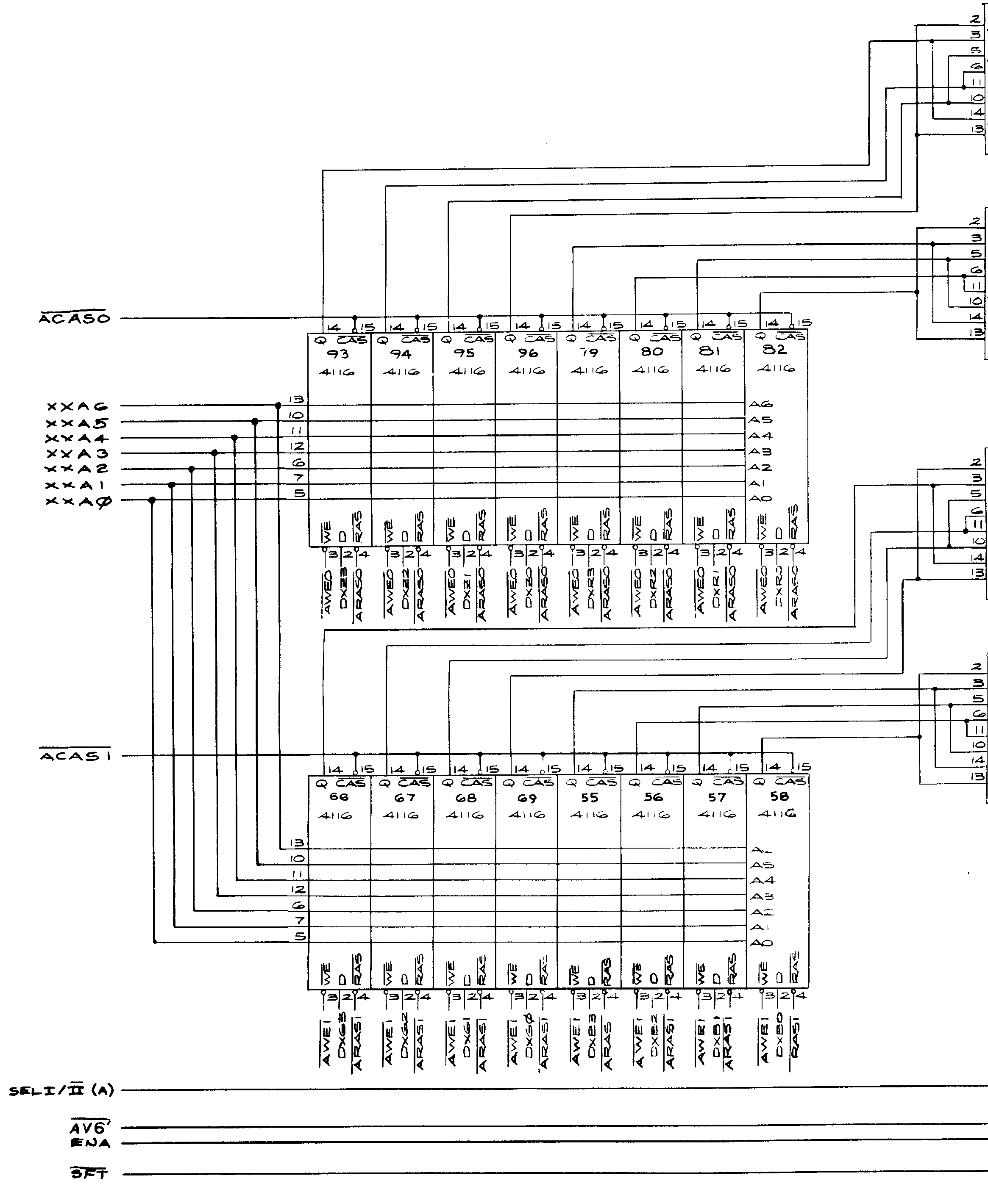
Dynamic RAM Control Latches

Playfield (Dynamic RAM A)

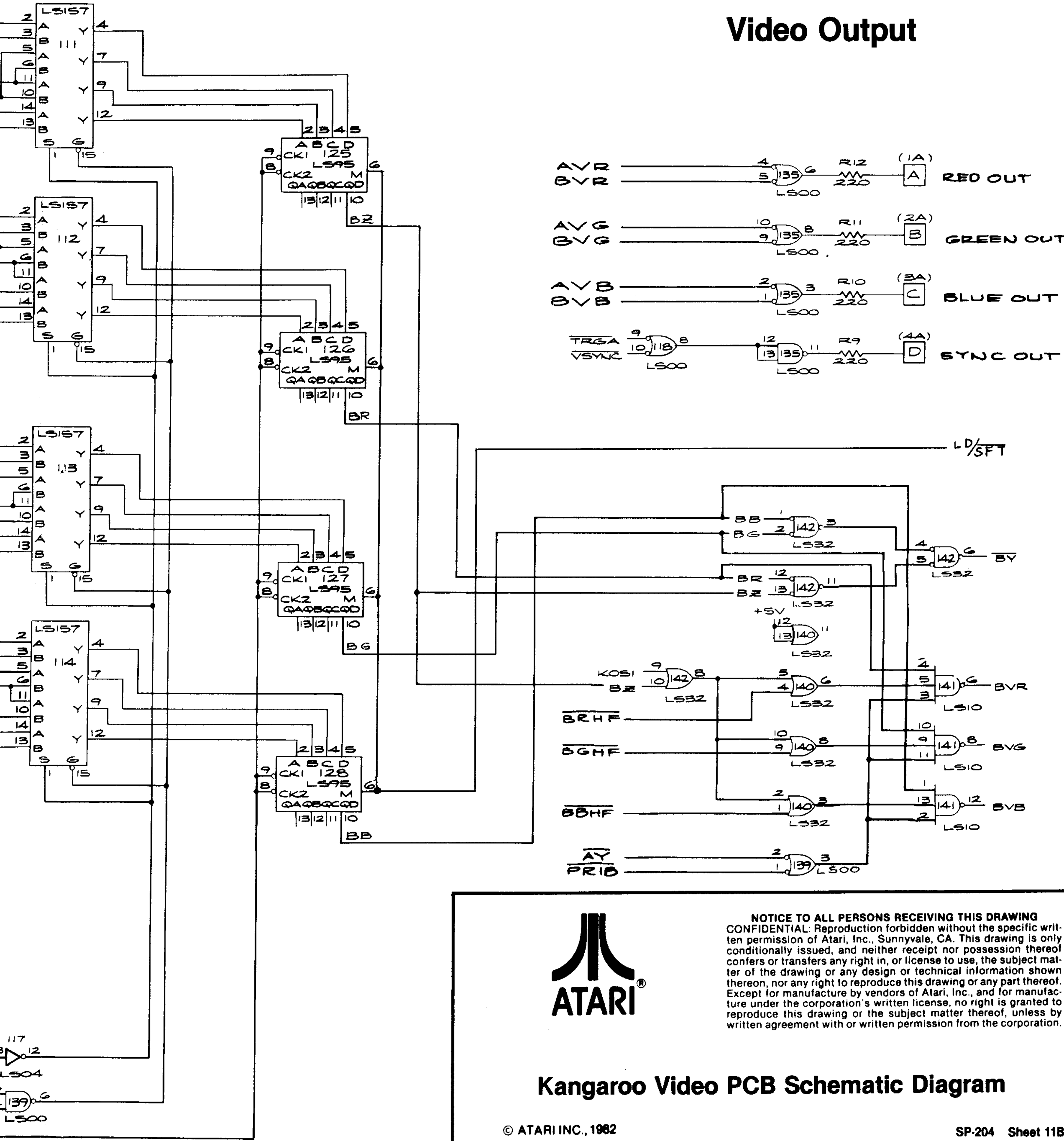


Kangaroo Video PCB Schematic Diagram

SP-204 Sheet 11A
3rd printing


ACASO
ACAS1
XXA6
XXA5
XXA4
XXA3
XXA2
XXA1
XXAØ
93
94
95
96
79
80
81
82
66
67
68
69
55
56
57
58
4116
SEL I/II (A)
AV6'
ENA
SFT

Video Output



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Kangaroo Video PCB Schematic Diagram

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SP-204 Sheet 11B
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Motion Object (Dynamic RAM B)

